EE 505

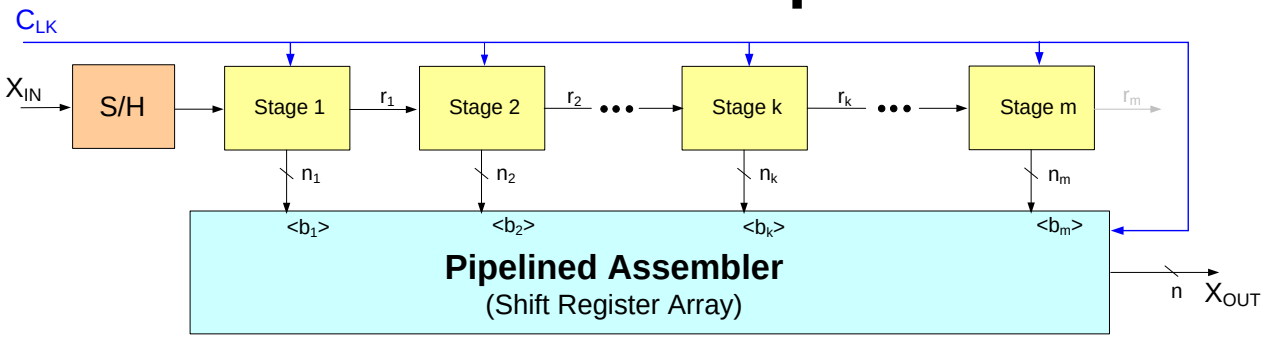
Lecture 26

ADC Design

- Pipeline
  - Noise
  - Switch Sizing
  - Bootstrapped Switches
  - Aperature Uncertainty

Review from last lecture

Power Dissipation



Capacitor sizing to meet noise requirements

For each stage: $P=[V_{SUP} \bullet GB \bullet C_L][V_{EB}]$

Should capacitor area be allocated to put dominant noise on input stage or later stages?

If part of the total noise comes from latter stages, size of capacitors on input stage can be reduced

An optimal noise distribution strategy should be followed!

Review from last lecture

Figure of Merit for Comparing Energy Efficiency of Op Amps

For Single-stage MOS implementation (with ref FD op amp or telescopic cascade op amp)

$$GB = \left[\frac{2 \bullet P}{V_{DD} C_L}\right] \left[\frac{1}{V_{EB}}\right]$$

Architecture Independent

Architecture Dependent

$$FOM = \frac{GB \bullet V_{SUP} C_L}{2P}$$

$$FOM_{\text{"Generic MOS Cascode-Type OpAmp"}} = \left[\frac{1}{V_{EB1}}\right]$$

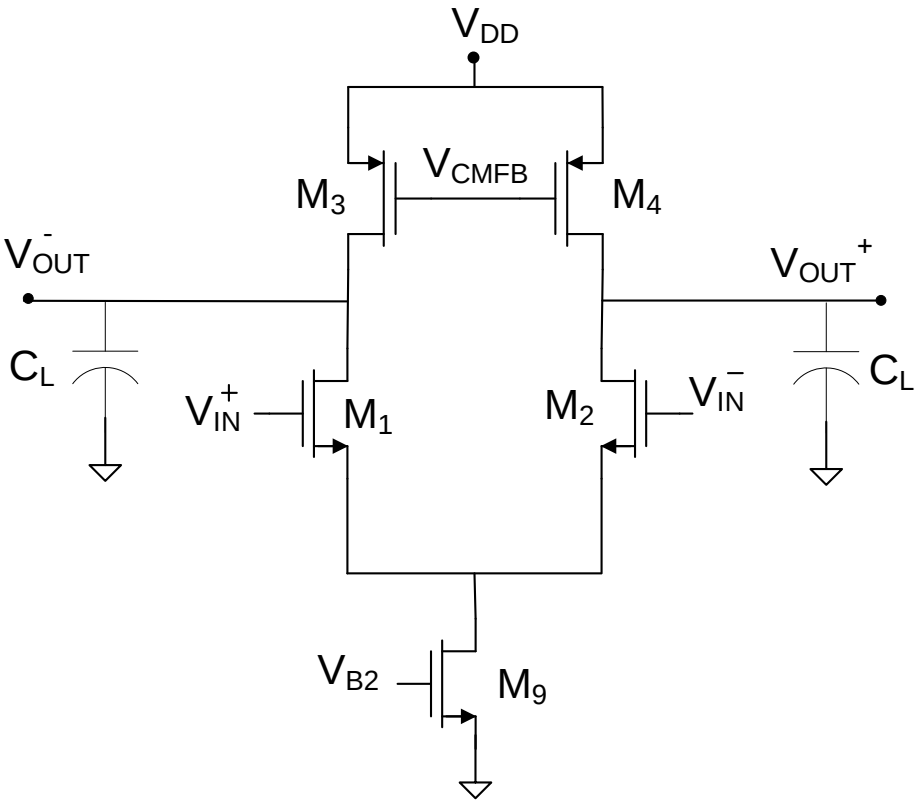
Review from last lecture

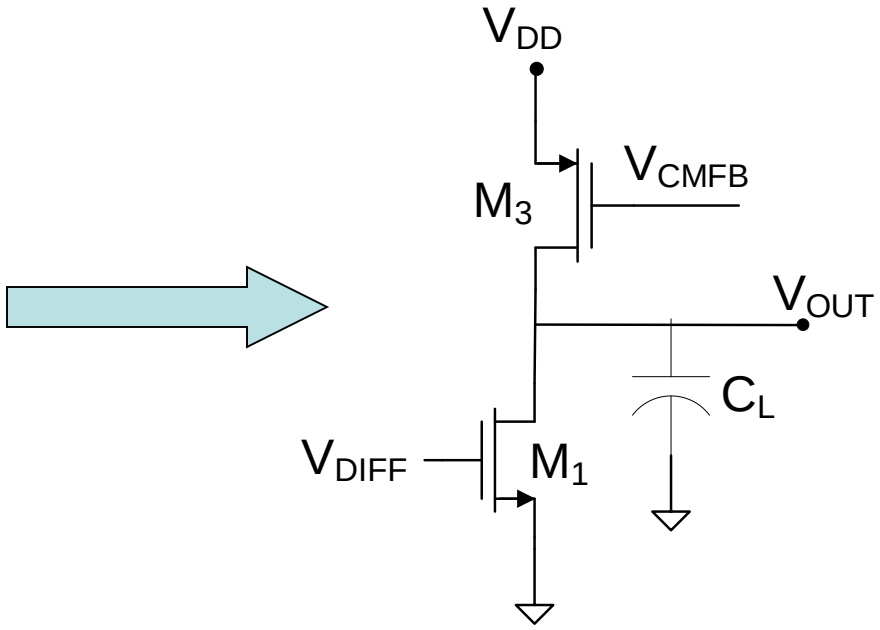
Energy Efficiency of Popular Single-Stage Op Amps

- Basic Single-Stage Diff Amp
- Current Mirror Op Amp
- Telescopic Cascode
- Folded Cascode
- Gain-Boosted Telescopic Cascode
- Gain-Boosted Folded Cascode
- -gm Compensated Single-Stage
- Telescopic Cascode Positive Feedback

Review from last lecture

Basic Single-Stage FD Op Amp





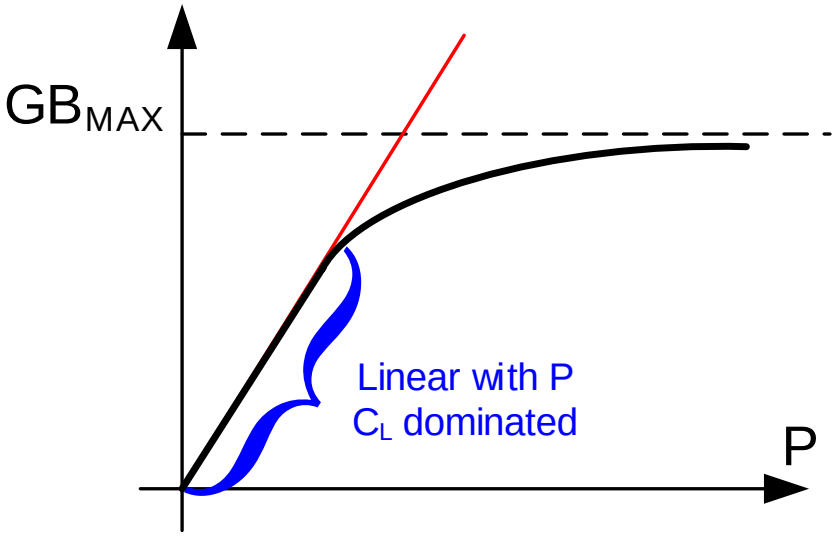
$$FOM = \left[\frac{1}{V_{EB1}}\right]$$

C_L on other output Not Shown

CMFB Not Shown

Review from last lecture

Is the linear settling time proportional to the reciprocal of the power even if parasitics are considered?



No – reach a point of diminishing returns as power is increased

GB_{MAX} independent of C_L

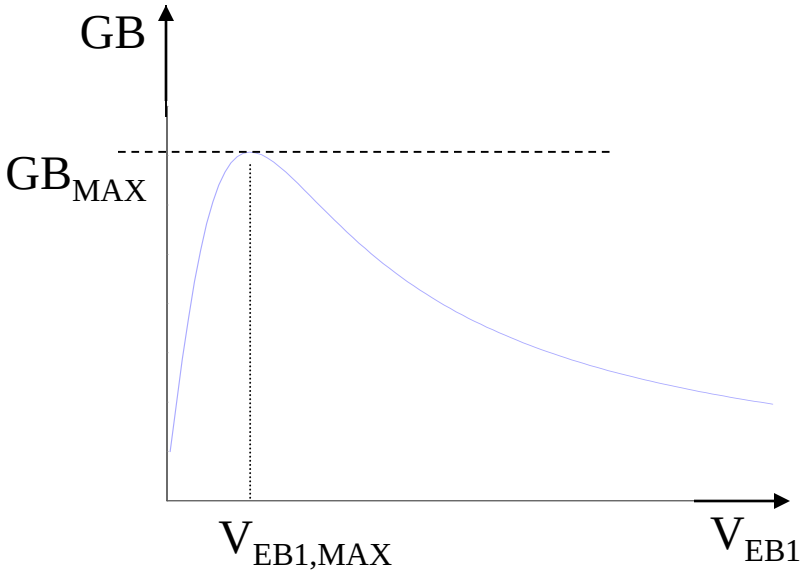
What is a practical point of diminishing returns?

$$GB_{CRIT} = \frac{GB_{MAX}}{2} = \frac{1}{4\left[\frac{L_{MIN}^2}{\mu_n V_{EB1}} C_{Xn} + \frac{V_{EB1} L_{MIN}^2}{\mu_p V_{EB3}^2} C_{Xp}\right]}$$

Review from last lecture

Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?

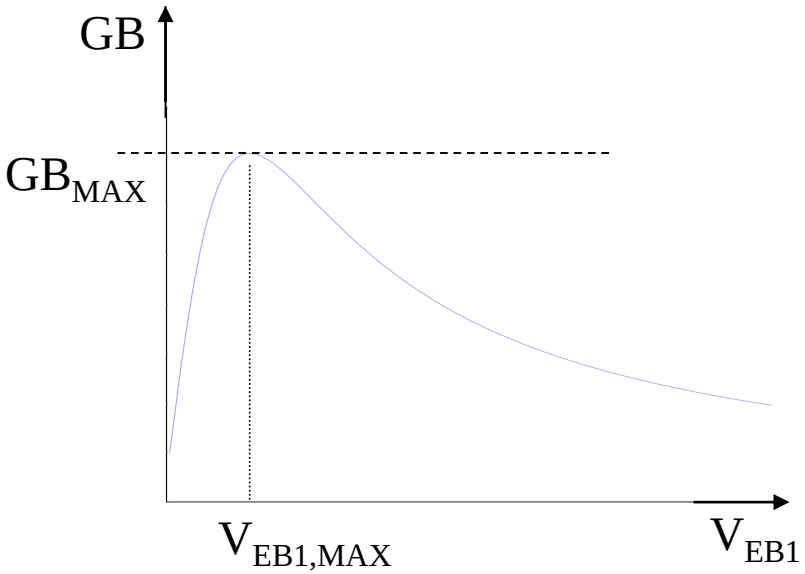
No – but an optimal value of V_{EB1} can be obtained



$$V_{EB1,MAX} = \sqrt{\frac{1}{\frac{C_L + 2d_1\left(C_{SWp} + C_{SWn}\right)}{\frac{P}{V_{DD}}\frac{L_{MIN}^2}{\mu_n}C_{Xn}} + \left[\frac{\mu_n C_{Xp}}{\mu_p C_{Xn} V_{EB3}^2}\right]}}$$

Review from last lecture

Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?



For large P, obtain

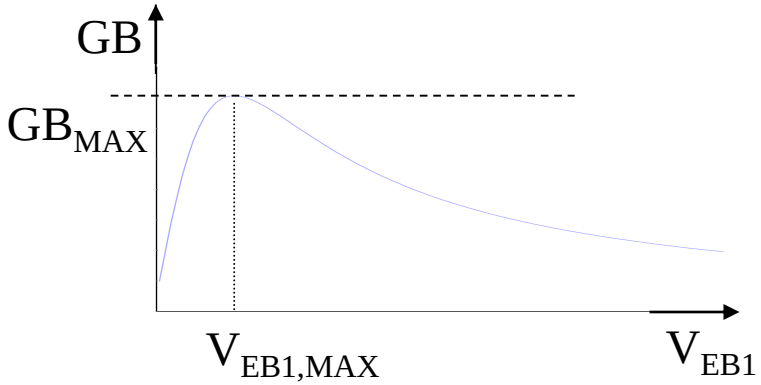
$$V_{EB1,MAX} = V_{EB3}\sqrt{\frac{\mu_p C_{Xn}}{\mu_n C_{Xp}}}$$

Substituting into GB_{MAX} expression, obtain

$$GB_{MAX} = \frac{\sqrt{\frac{\mu_n \mu_p}{C_{Xn} C_{Xp}}}\, V_{EB3}}{4L_{MIN}^2} = \frac{\omega_{Tp}}{4\sqrt{C_{Xn} C_{Xp}}}\sqrt{\frac{\mu_p}{\mu_n}}$$

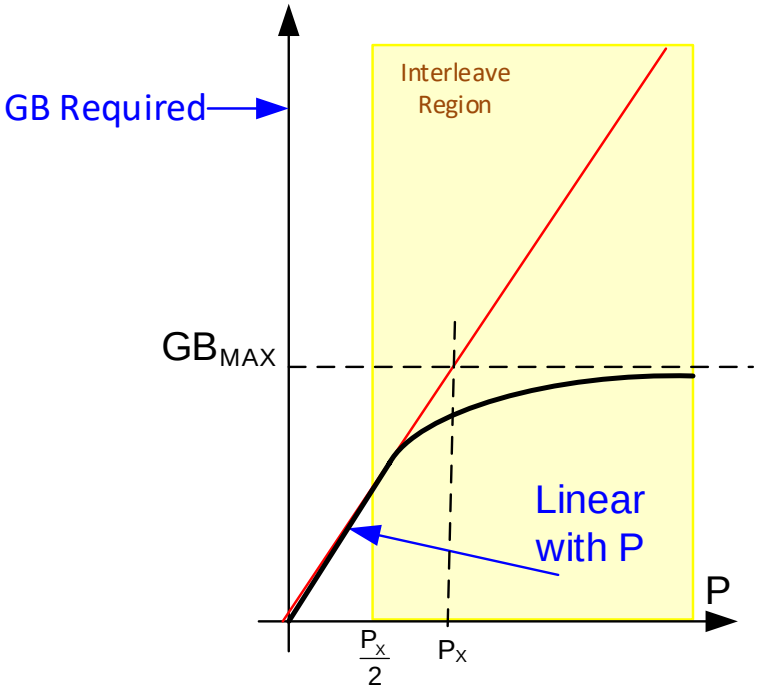
Review from last lecture

Is the strategy of minimizing V_{EB1} to minimize settling time justifiable even if parasitics are considered?



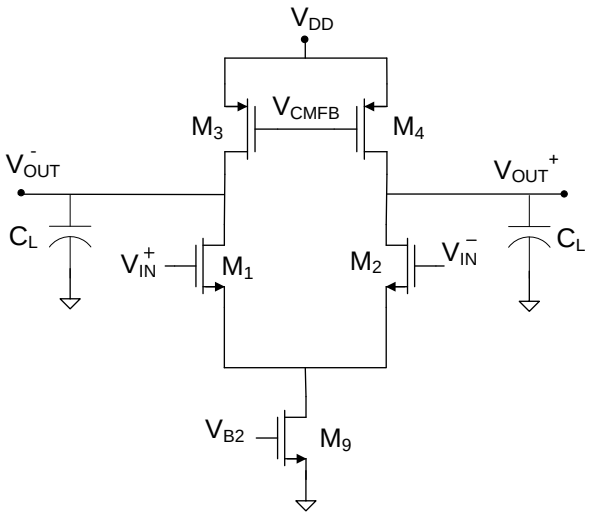
$$GB_{MAX} = \frac{\omega_{Tp}}{4\sqrt{C_{Xn}C_{Xp}}}\sqrt{\frac{\mu_p}{\mu_n}}$$

If GB_{MAX} is not high enough, interleaving may provide a viable solution in a given technology node

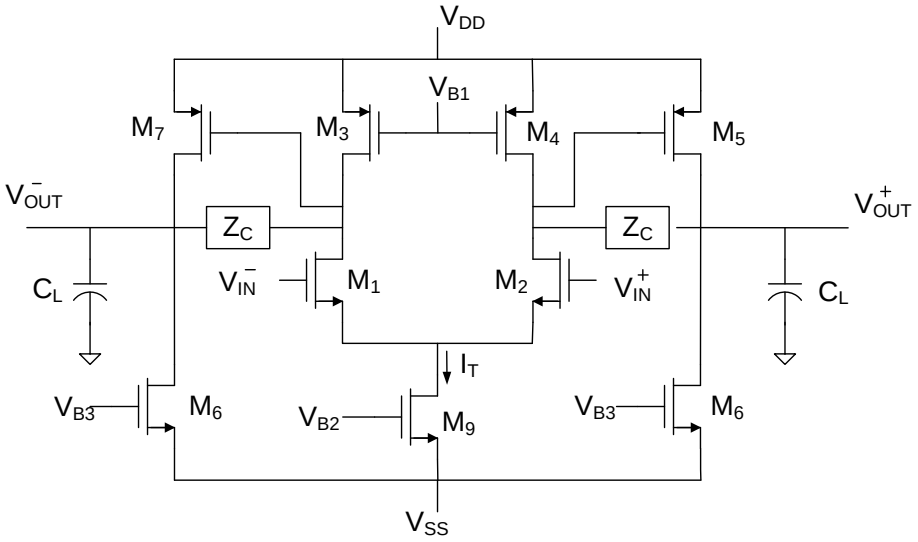


Review from last lecture

Improved Energy Efficiency Op Amps



OR ?



For some closed-loop gains the two-stage op amp is more power efficient than the single-stage Op Amp

See ISCAS 2005

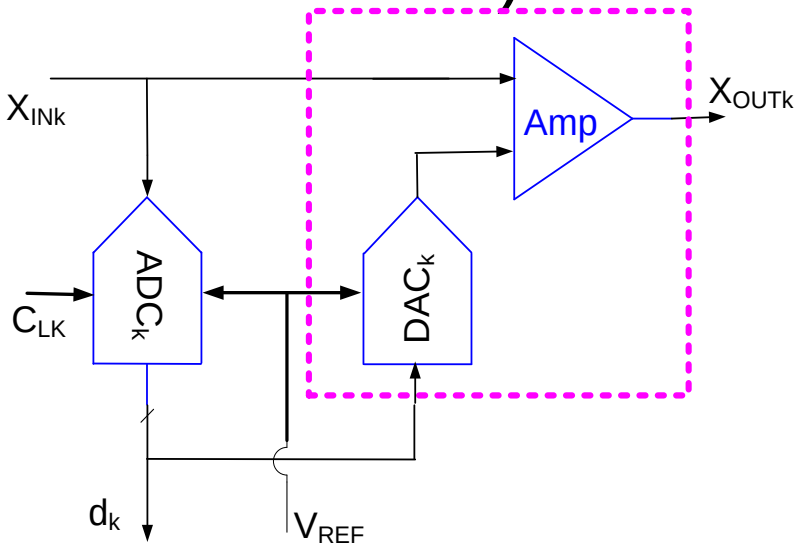
Power Dependence of Feedback Amplifiers on OpAmp Architecture

Vipul Katyal, Yu Lin and Randall L. Geiger

Performance Limitations

(consider amplifier, ADC and DAC issues)

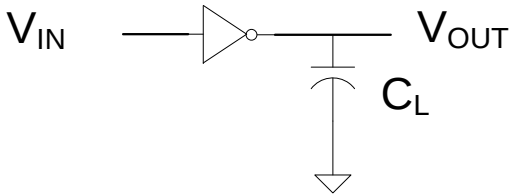
- ADC
  - Break Points (offsets)
- DAC
  - DAC Levels (offsets)
    - Out-range (over or under range)
- Amplifier
  - Offset voltages
  - Settling Time
  - Nonlinearity (primarily open loop)
    - Open-loop
    - Out-range
  - Gain Errors
    - Inadequate open loop gain
      - Component mismatch
  - Power Dissipation
  - kT/C switching noise



I/O Power Dissipation

- Driving the output pads can consume considerable power

For a single bit line



$$P=f_{CL}V_{SUP}^{2}C_{L}$$

For an n-bit ADC

$$P=n\bullet f_{CL}V_{SUP}^{2}C_{L}$$

Example: if n=14, V_{SUP}=3.3V, C_L=5pF, f_{CL}=100MHz, 50% change

$$P=14\bullet 10^{8}\bullet\frac{1}{2}\bullet 3.3^{2}\bullet 5\text{E-}12=35\text{mW}$$

I/O Power Dissipation

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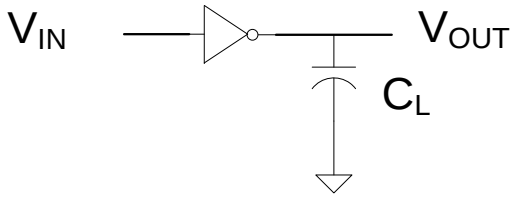
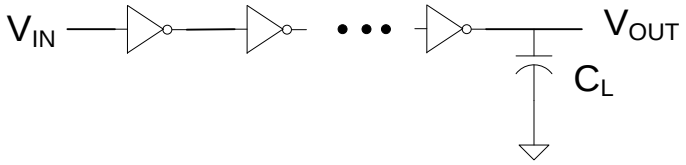


$$P = f_{CL} V_{SUP}^2 C_L$$



$$P \cong 2 f_{CL} V_{SUP}^2 C_L$$

For an n-bit ADC

$$P = n \bullet f_{CL} V_{SUP}^2 C_L$$

$$P = 2n \bullet f_{CL} V_{SUP}^2 C_L$$

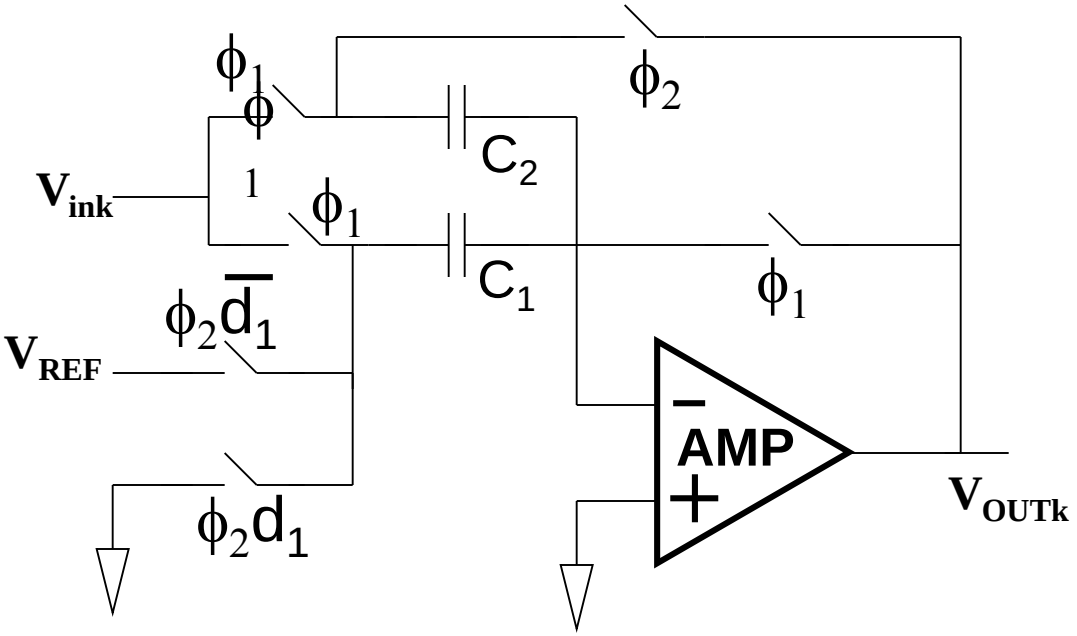
Example: if n=14, V_{SUP}=3.3V, C_L=5pF, f_{CL}=100MHz, 50% change

P=35mW

$P \cong 70mW$

Interstage Amplifiers

Typical Finite-Gain Inter-stage Amplifier
(shown single-ended with 1-bit/stage)



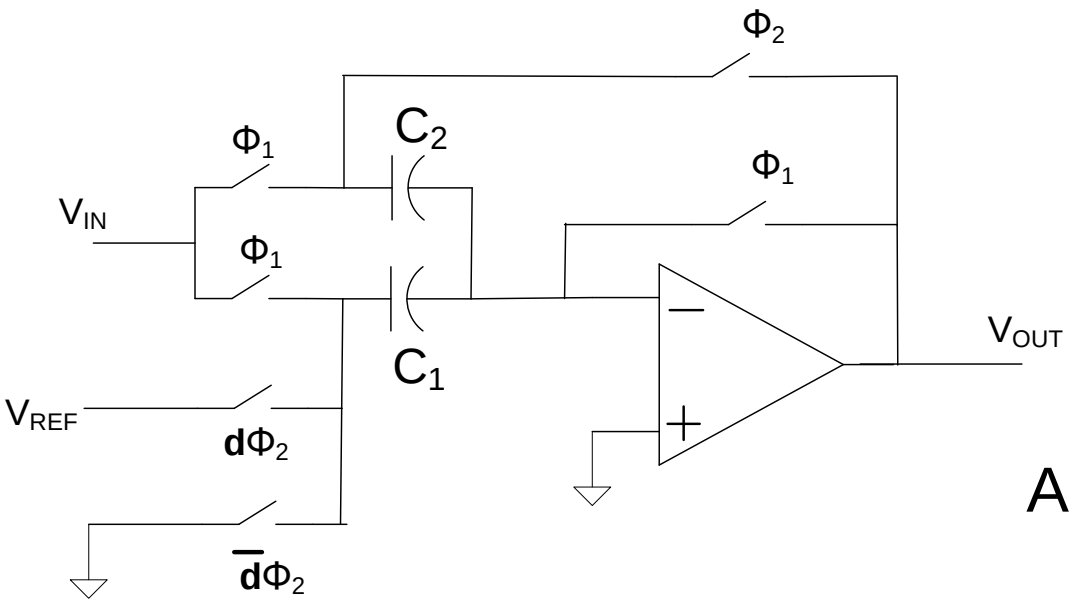
Ideally

$$V_{OUT} = V_{IN}\left(1+\frac{C_1}{C_2}\right) - d_1\left(\frac{C_1}{C_2}\right)V_{REF}$$

$$V_{OUT} = 2V_{IN} - d_1 V_{REF}$$

Gain =2.00000

Clock Phasing and Clock Generation



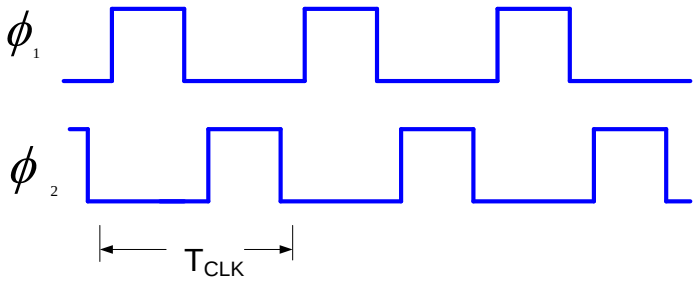
$$\beta_2 = \frac{C_2}{C_1 + C_2}$$

$$\beta_1 = 1$$

$$A_{FB2} = 1 + \frac{C_2}{C_1} = \frac{1}{\beta_2}$$

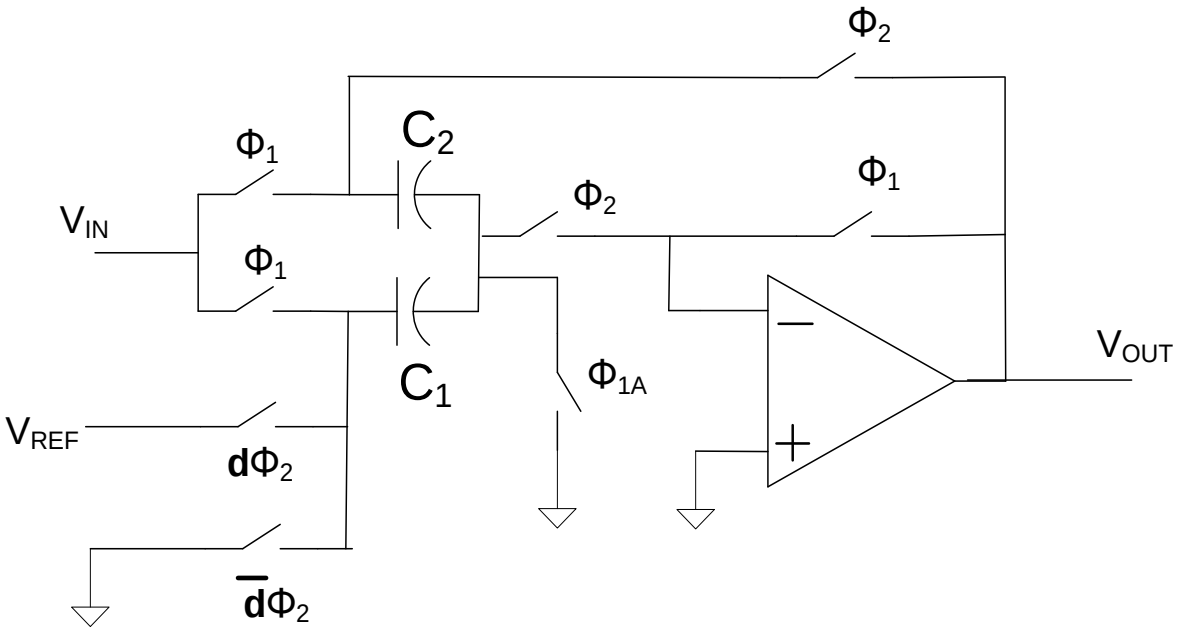
Signal-dependent Sampling Seriously Degrades Linearity if V_{IN} is not constant during sampling

Boot-strapping sampling or bottom-plate sampling needed



Flip-Around Amplifier

Clock Phasing and Clock Generation



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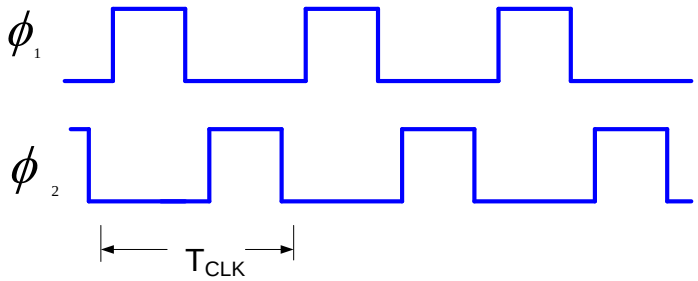
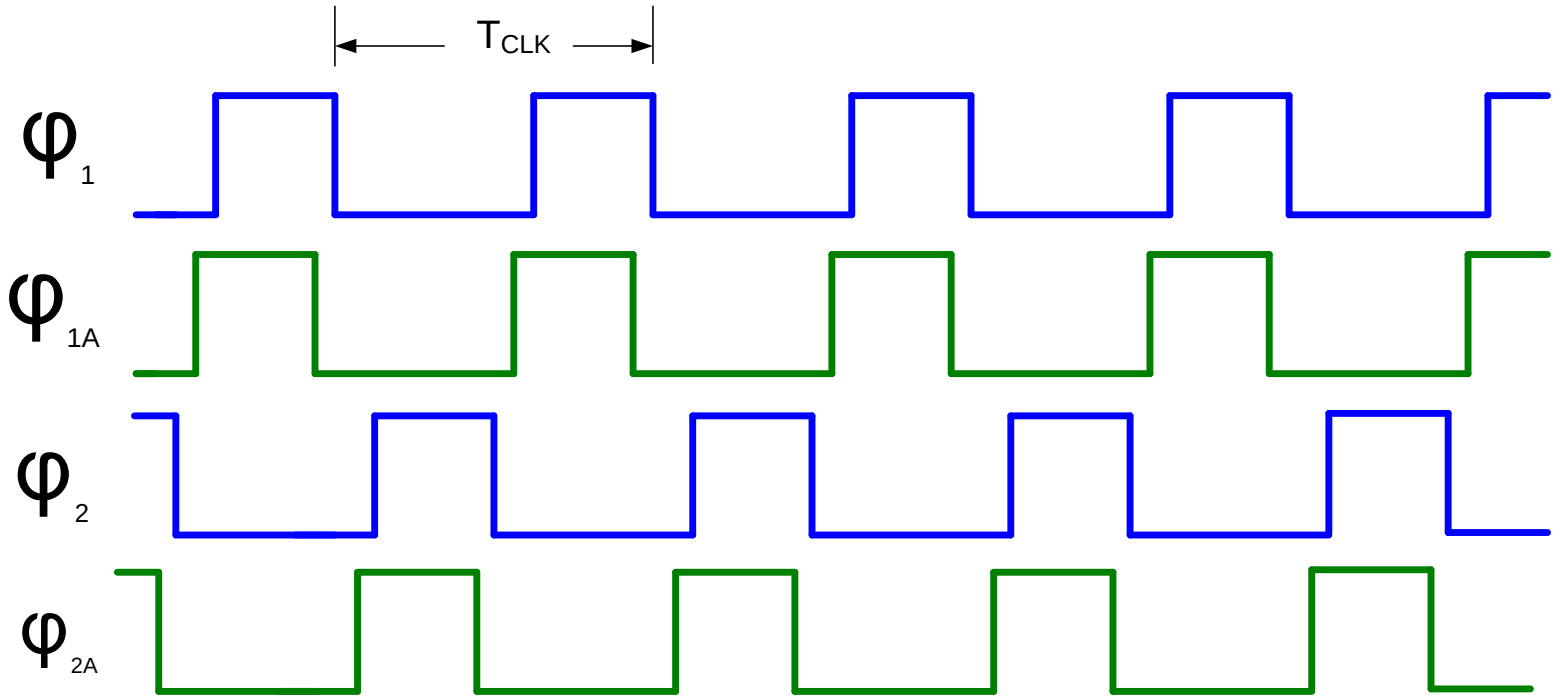


Bottom-Plate Sampling

Must advance φ_1 if V_{IN} is not constant

Flip-Around Amplifier

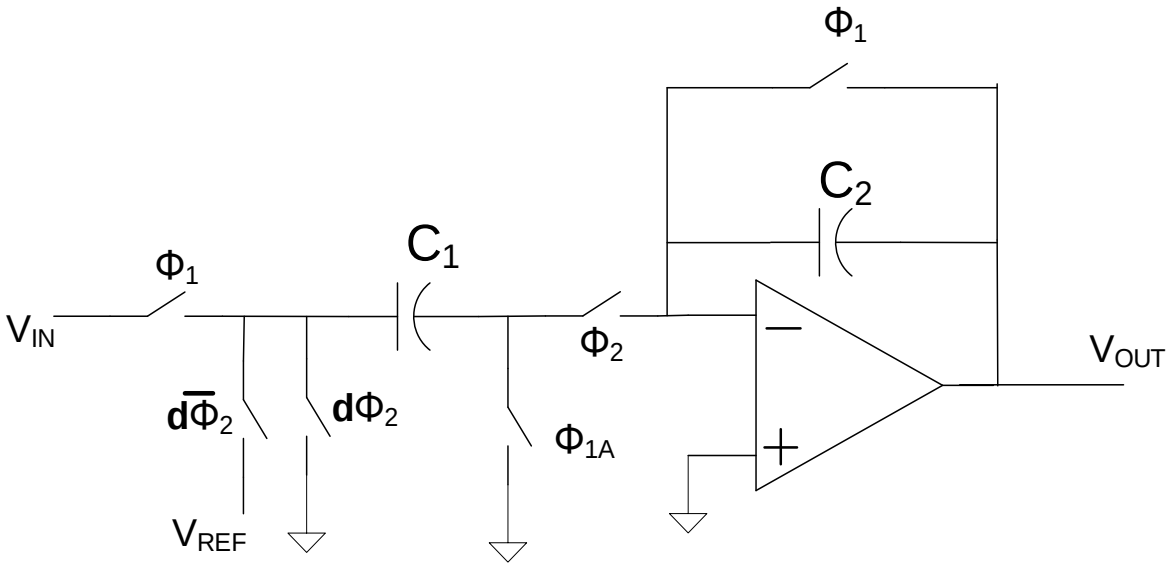
Clock Phasing and Clock Generation



Flip-Around Amplifier Clock Timing

Reduces Sampling noise if quiet when φ_{1A} transitions

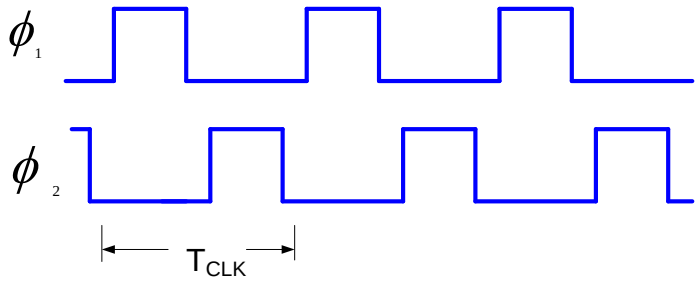
Clock Phasing and Clock Generation



$$\beta_2 = \frac{C_2}{C_1 + C_2}$$

$$\beta_1 = 1$$

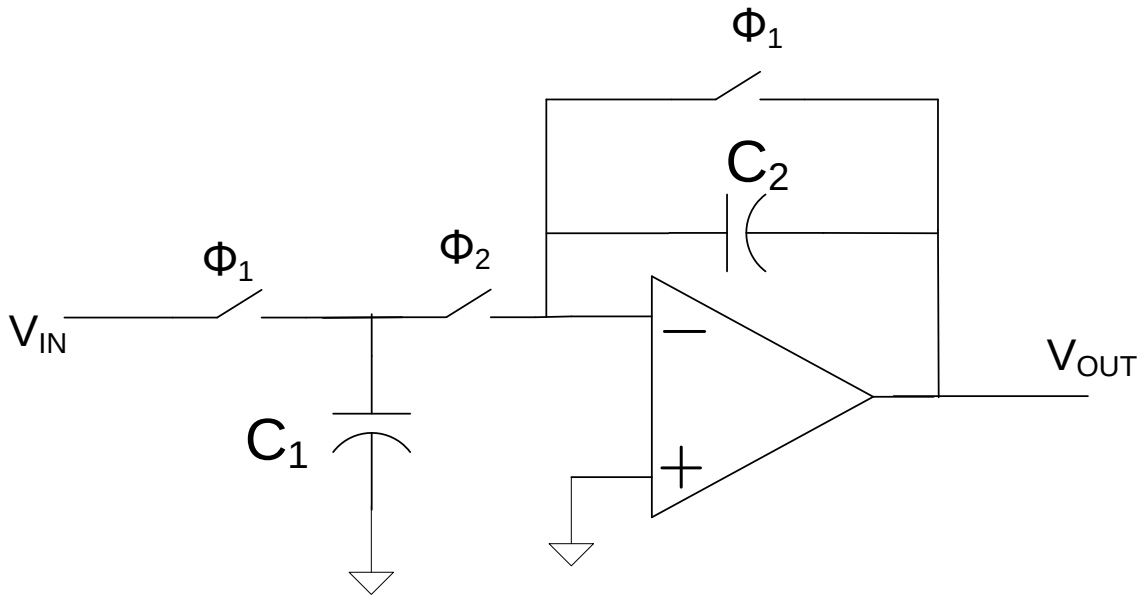
$$A_{FB2} = \frac{C_2}{C_1} \neq \frac{1}{\beta_2}$$

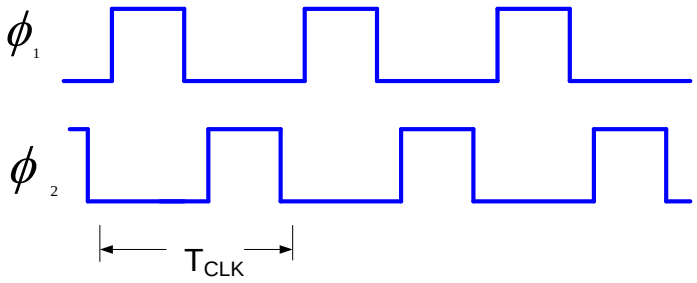


Must advance φ_1 if V_{IN} is not constant

Popular SC Amplifier

Clock Phasing and Clock Generation





Parasitic Sensitive

Signal-dependent delays

Clock Phasing and Clock Generation

How is GB determined?

$$GB_{RPS} \cong \frac{2\ln(2)(n_{ST}+1)}{\beta_{MIN}} f_{CLK}$$

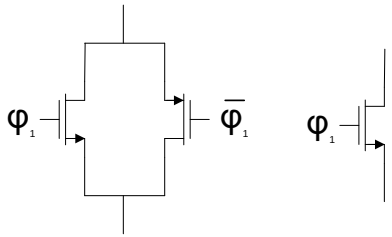
(to settle to ½ LSB derived in Lecture 24)

How are switches sized?

$$R_{SW} = \frac{1}{Cf_{CLK}\,2\ln(2)(n_{ST}+1)}$$

(to settle to ½ LSB – will be derived later)

May need to use TG switch if large signals present but prefer to avoid !



Pipelined Data Converter Design Guidelines

Issue	Strategy
1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if α_k's correctly interpreted a) Use Extra Comparators b) Use sub-radix structures
2. Op Amp Gain causes finite gain errors and introduces noninearity	2. a) Select op amp architecture that has acceptable signal swing b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors
3. Op amp settling must can cause errors	3. Select GB to meet settling requirements (degrade modestly to account for slewing)
4. Power dissipation strongly dependent upon GB of Op Amps	4. Minimize C_L, use energy efficient op amps, share or shut down op amp when not used,scale power in latter stages, eliminate input S/H if possible, interleave at high frequencies. Good (near optimal) noise distribution strategy should be followed.
5. Choice of FB Amplifier Architecture seriously impacts performance	5. Bottom plate sampling, bootatrapping, clock advance to reduce aperature uncertainty,critical GB, parasitic insensitivity needed, β dependent upon architecture and phase, compensation for worst-case β, TG if needed

Have probably not included the most important issue in these guidelines:

Pipelined Data Converter Design Guidelines

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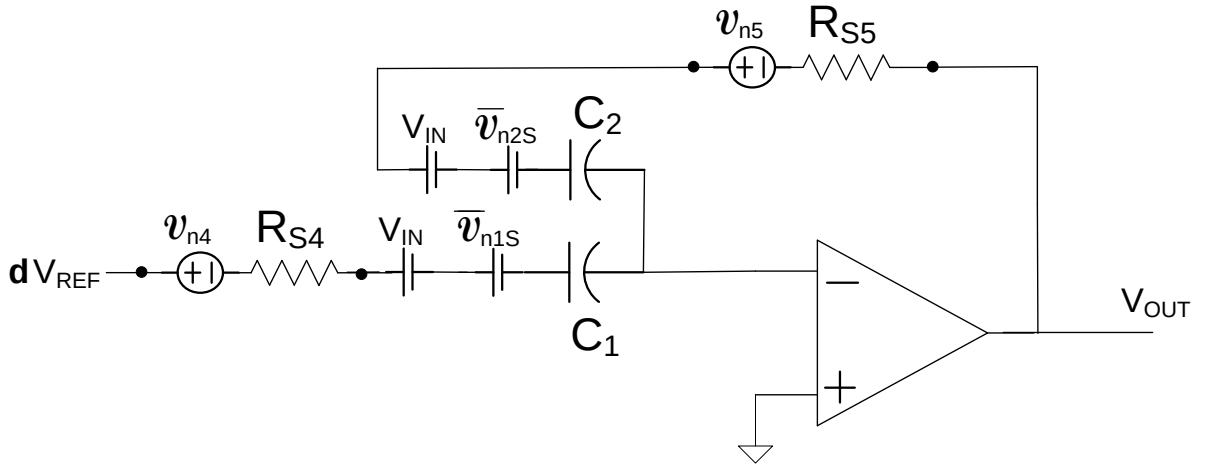
6. Correct interpretation of α_k's is critical	6. a) Accurately set α_k values b) Use analog or digital calibration

Review

Sampling Noise



$$\beta_2 = \frac{C_2}{C_1 + C_2}$$

If the ON impedance of the switches is small and it is assumed that $C_1=C_2=C$, $R_{S4}=R_{S5}=R_{SW}$, it can be shown that for $C_1=C_2$

$$\hat{v}_{IN\text{-}RMS} = \sqrt{\frac{kT}{2C} + \frac{kT}{4} R_{SW} GB}$$

Too much GB or too large of R_{SW} can increase sampled noise voltage

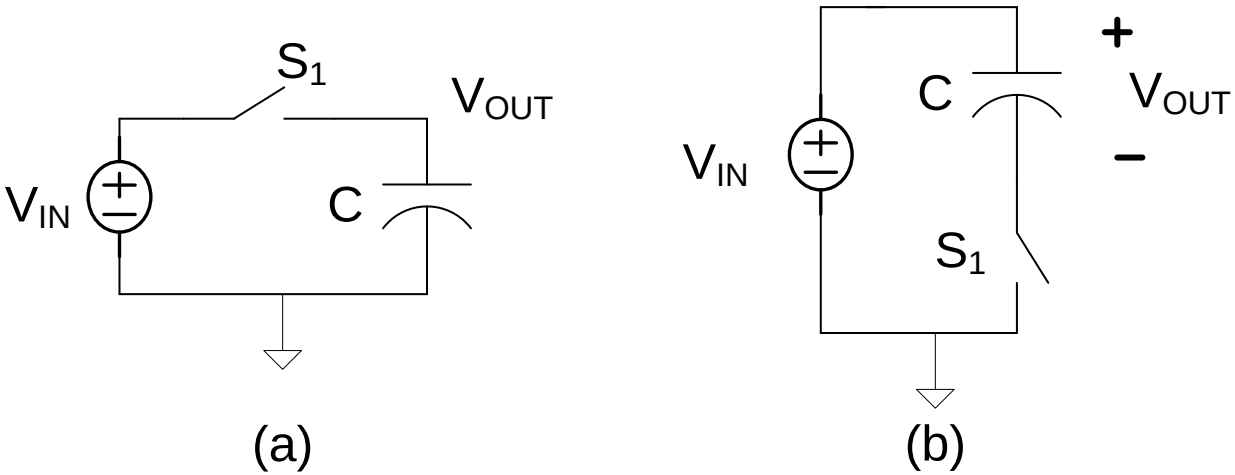
Too small of R_{SW} will not derive any benefit and will increase power, area, and driving problems

GB must be large enough to have complete settling

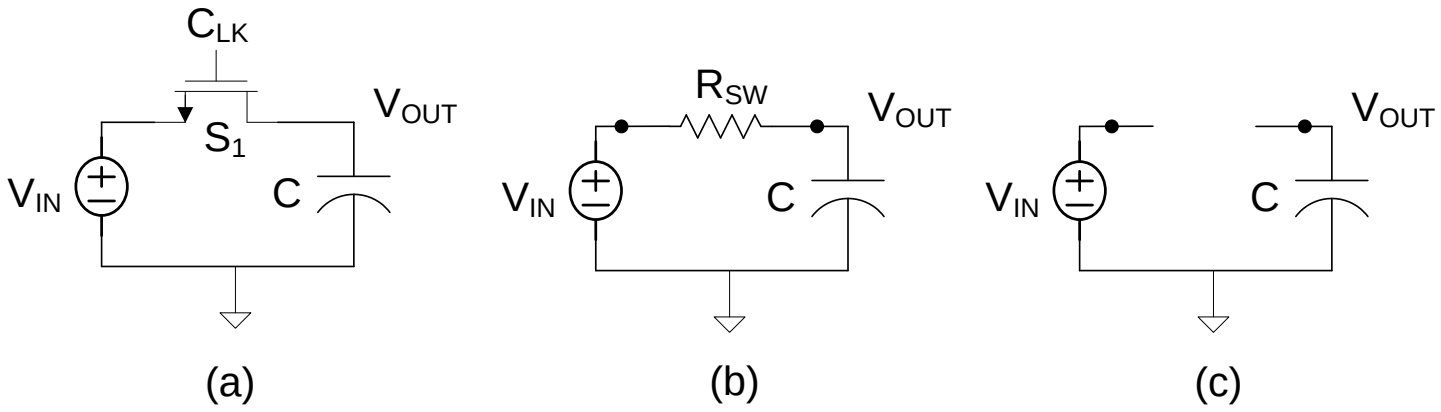
Sampling Noise

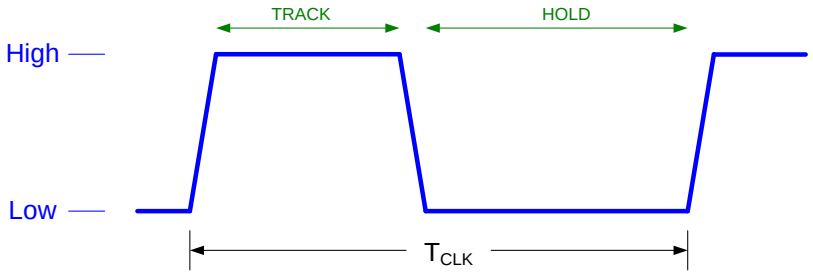
- Capacitors introduce no noise
- Noise is, however, present in switches that take samples
- This switch noise causes SNR problems in the amplifier if not correctly managed

Sampling Noise

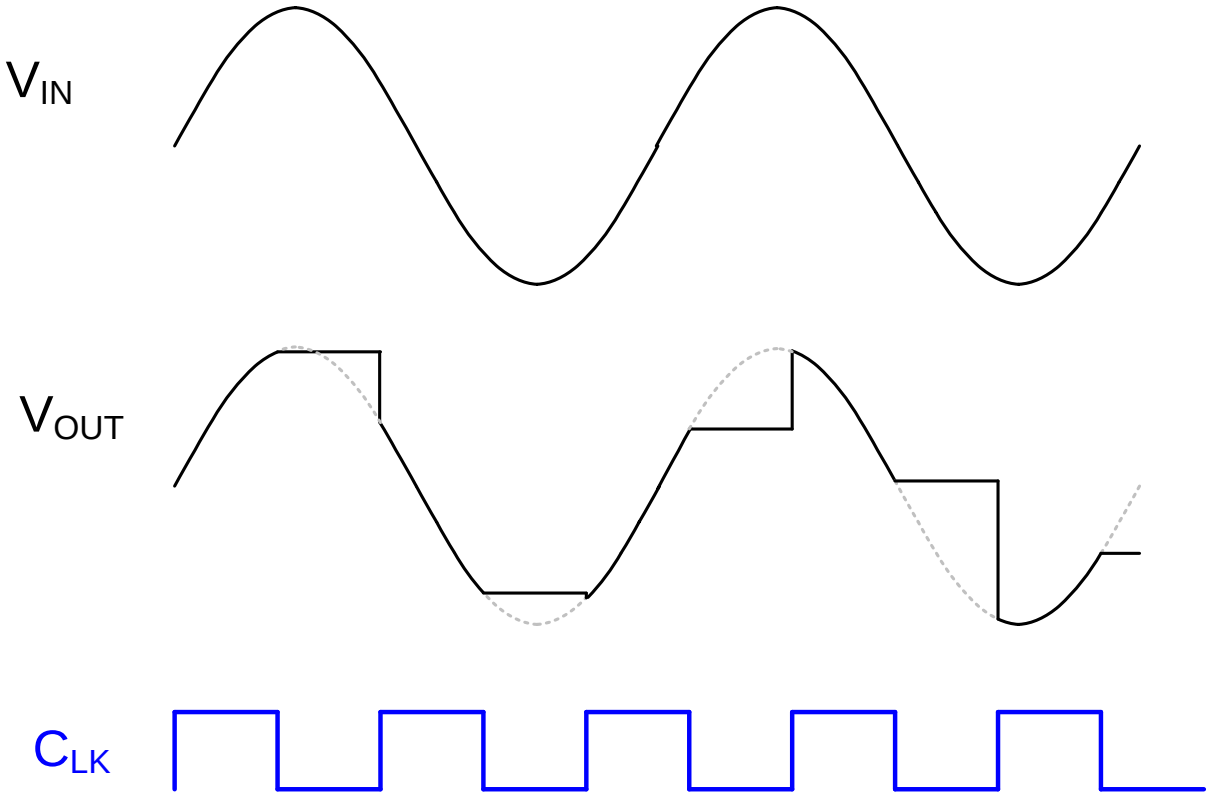


Sampling Noise

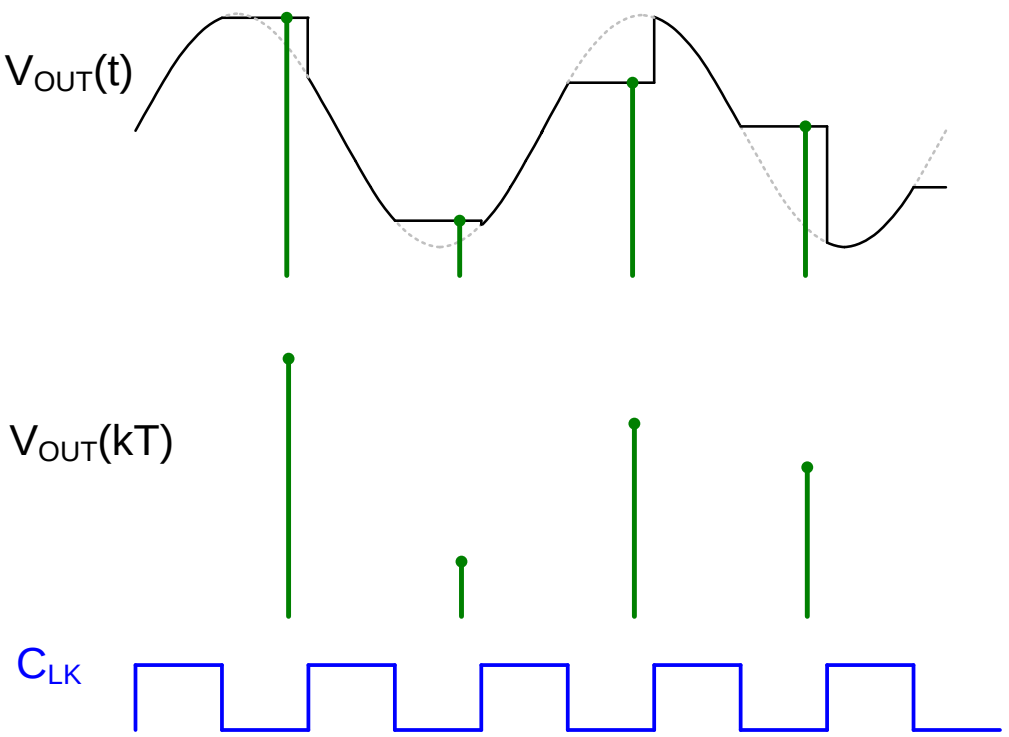




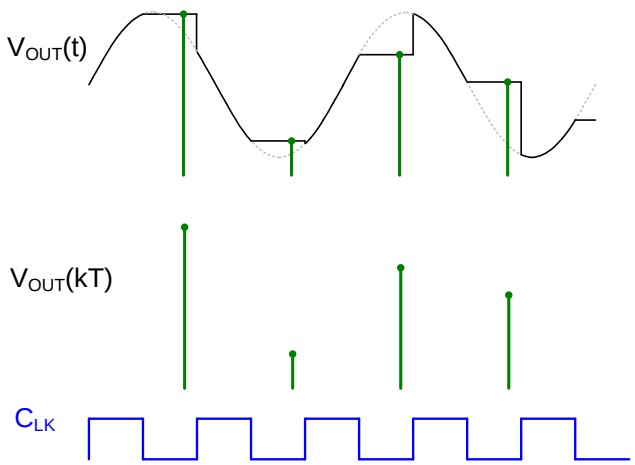
Sampling Noise

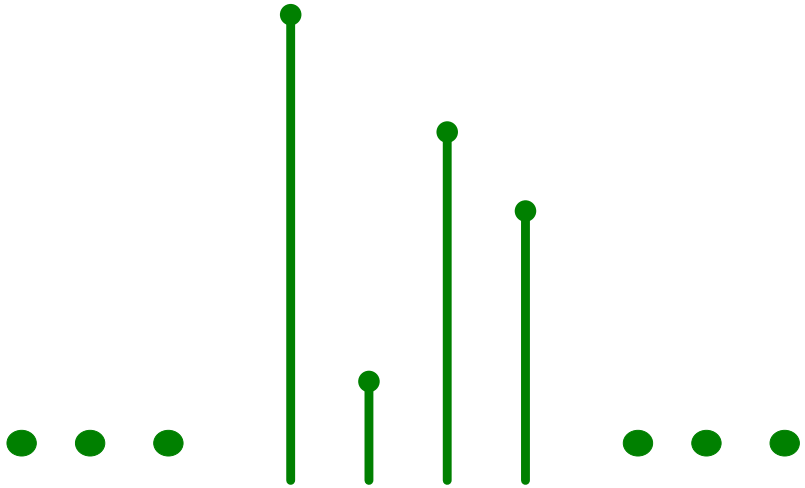


Sampling Noise

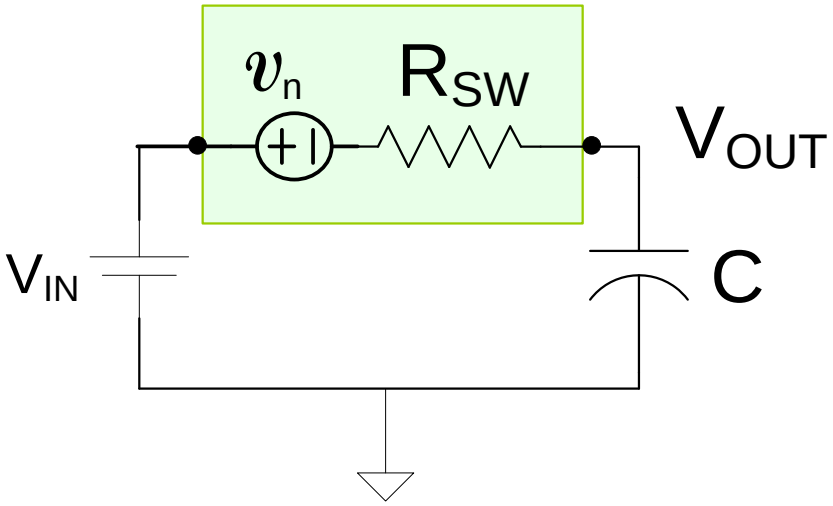


Sampling Noise





Sampling Noise

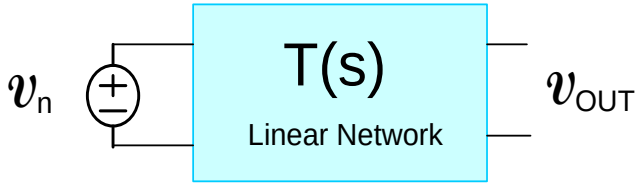


Power spectral density of any resistor, R_{SW}, is given by

$$S_{VR} = 4kTR_{SW}$$

This is thermal noise and often termed “white” noise since the spectral dissipation is uniform for all f

Sampling Noise



Theorem 1 If $v_n(t)$ is a continuous-time zero-mean noise source with power spectral density S_V, then the spectral density of v_{OUT} is given by the expression

$$S_{V_{OUT}} = \left|T(s)\right|^2_{s=j\omega} S_V$$

The RMS value of a continuous-time random variable V(T) is defined to be

$$V_{RMS} = E\left(\sqrt{\lim_{T\to\infty}\left(\frac{1}{T}\int_0^T V^2(t)dt\right)}\right)$$

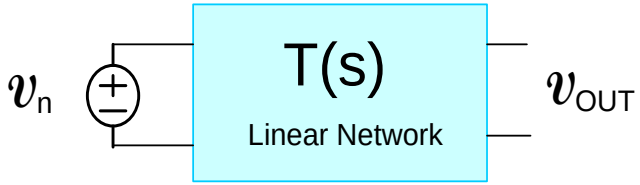
The RMS value of a random sequence <V(kT)> is defined to be

$$\hat{V}_{RMS} = E\left(\sqrt{\lim_{N\to\infty}\left(\frac{1}{N}\sum_{k=1}^{N} V^2(kT)\right)}\right)$$

(the operator E is the expected value operator)

(these definitions apply to non-random signals as well)

Sampling Noise



Theorem 1 If $v_n(t)$ is a continuous-time zero-mean noise source with power spectral density S_V, then the spectral density of v_{OUT} is given by the expression

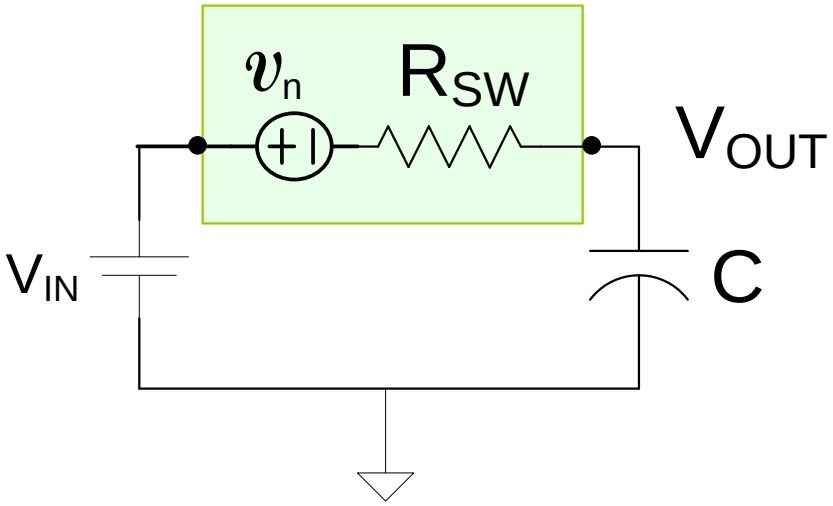
$$S_{V_{OUT}} = \left|T(s)\right|^2_{s=j\omega} S_v$$

Theorem 2 If $v(t)$ is a continuous-time zero-mean noise voltage with power spectral density S_V, then the RMS value of the continuous-time noise is given by

$$V_{RMS} = \sqrt{\int_{f=0}^{\infty} S_v \, df}$$

Note: There are some parts of the hypothesis of this theorem that have not been stated such as stationary of the distribution and no correlation between samples spaced T seconds apart..

Sampling Noise

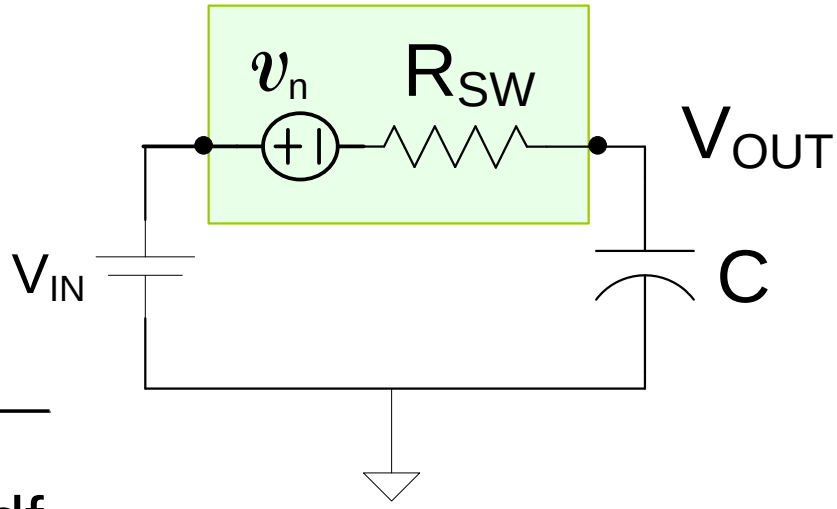


$$S_{VR} = 4kTR_{SW}$$

$$S_{VOUT} = 4kTR\left(\frac{1}{1+(RC\omega)^2}\right)$$

Sampling Noise

$$S_{VOUT} = 4kTR\left(\frac{1}{1+(RC\omega)^2}\right)$$



$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2R^2C^2}\,df}$$

Recall:

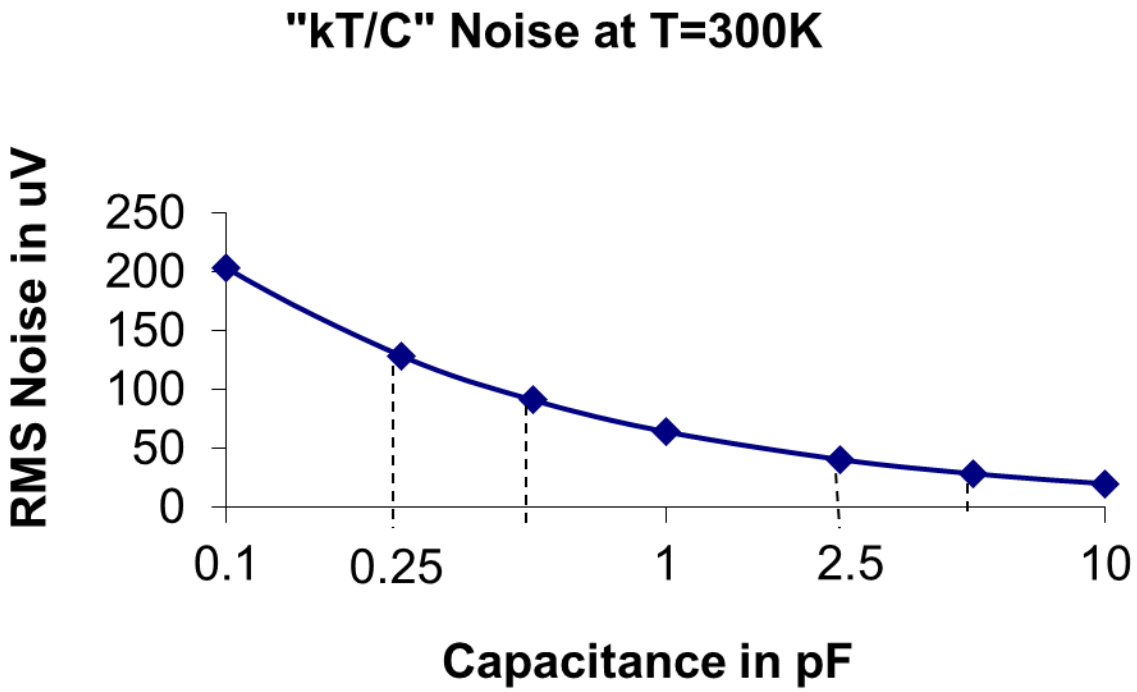
$$\int_{y=0}^{\infty} \frac{1}{1+y^2}\,dy = \left(\tan^{-1} y\right)\Big|_{y=0}^{\infty} = \frac{\pi}{2}$$

Change of variable: $z=\omega RC$, $dz=2\pi RC\,df$

$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,df} = \sqrt{\frac{kT}{C}}$$

Key Result, Continuous-time noise at V_{OUT}

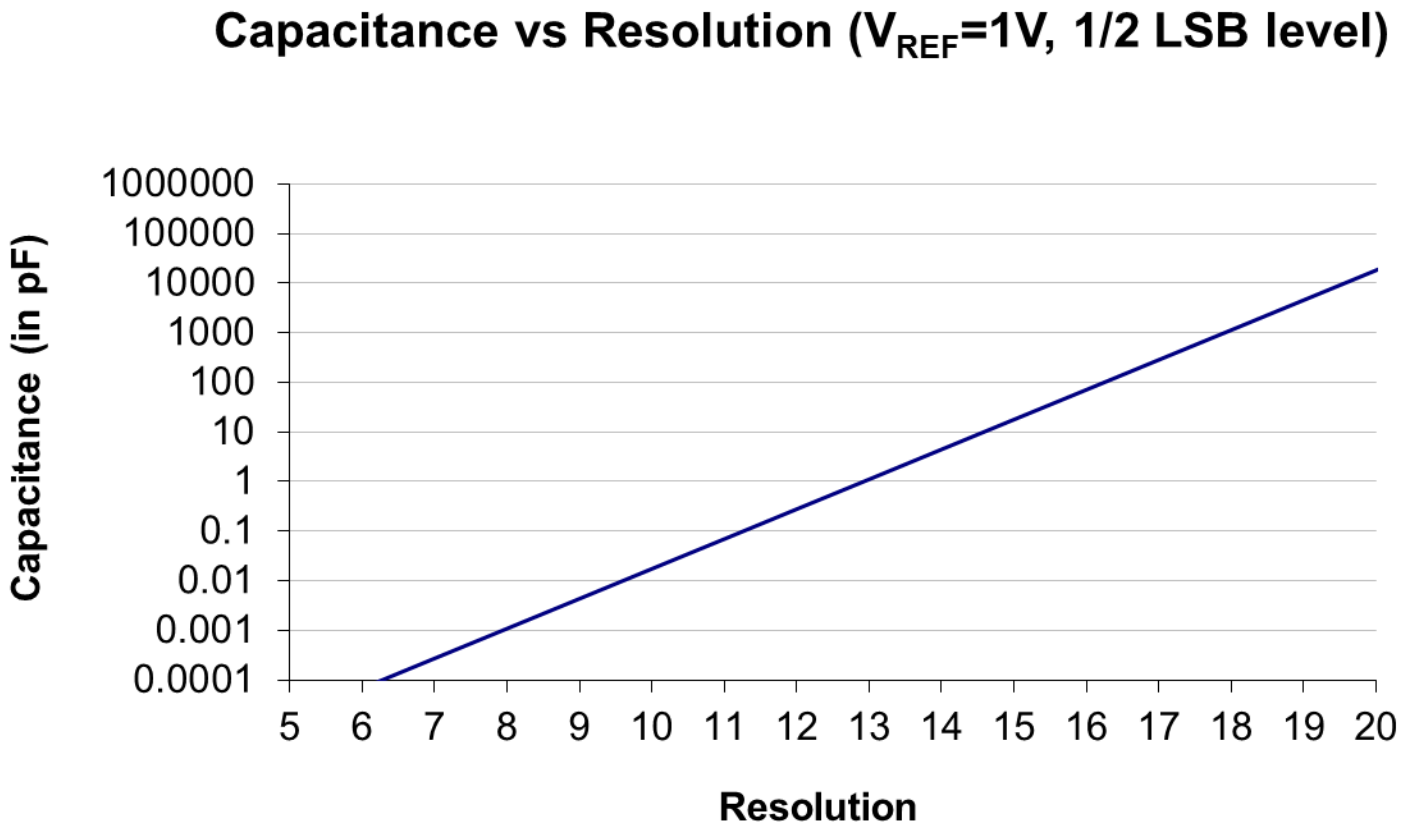
Sampling Noise



- Since noise is independent of V_{REF}, would like to make V_{REF} as large as possible to minimize C sizing

- Scaling to lower supply voltage has a negative impact on capacitor sizing (scaling supply by 2 requires increasing C by factor of 4 to maintain SNR)

Sampling Noise



Example: 14-bit ADC C=4.6pF

Sampling Noise

Theorem 3 If V(t) is a continuous-time zero-mean noise voltage and <V(kT)> is a sampled version of V(t) sampled at times T, 2T, …. then the RMS value of the continuous-time waveform is the same as that of the sampled version of the waveform. This can be expressed as

$$V_{RMS} = \hat{V}_{RMS}$$

Note: There are some parts of the hypothesis of this theorem that have not been stated such as stationary of the distribution and no correlation between samples spaced T seconds apart..

Sampling Noise

.

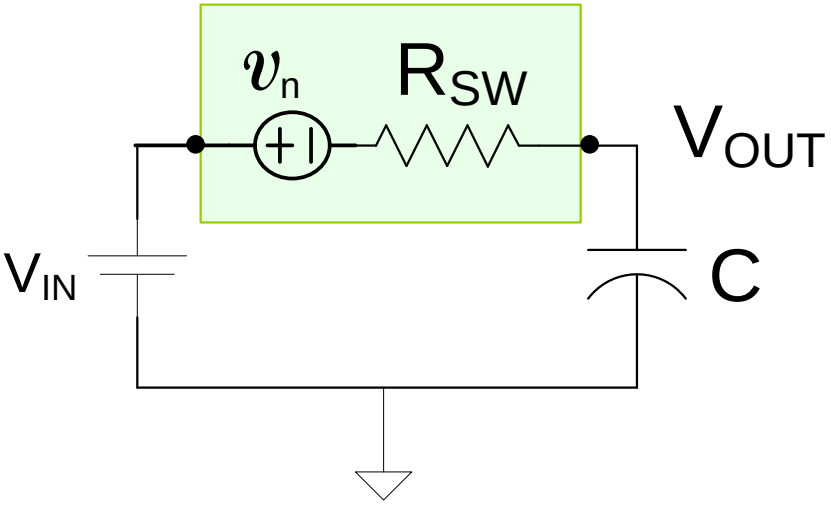
Theorem 4 If V(t) is a continuous-time zero-mean noise source and <V(kT)> is a sampled version of V(t) sampled at times T, 2T, …. then the standard deviation of the random variable V(kT), denoted as $\sigma_{\hat{V}}$ satisfies the expression

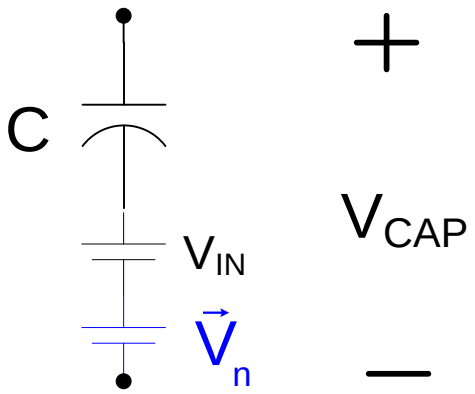
$$\sigma_{\hat{V}} = V_{RMS} = \hat{V}_{RMS}$$

Theorem 5 The RMS value and the standard deviation of the noise voltage that occurs in the basic switched-capacitor sampler is related to the capacitor value by the expression

$$\hat{V}_{RMS} = V_{RMS} = \sigma_{\hat{V}} = \sqrt{\frac{kT}{C}}$$

Sampling Noise





$$v_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

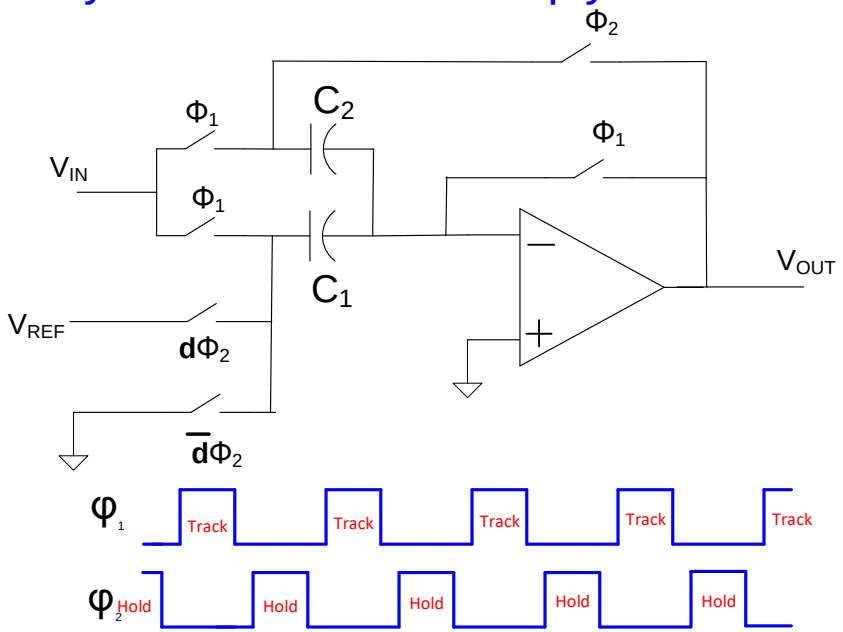
$$\hat{v}_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

Key Result, Continuous-time noise at V_{OUT}

Key Result, Discrete-time noise at V_{OUT}

Sampling Noise

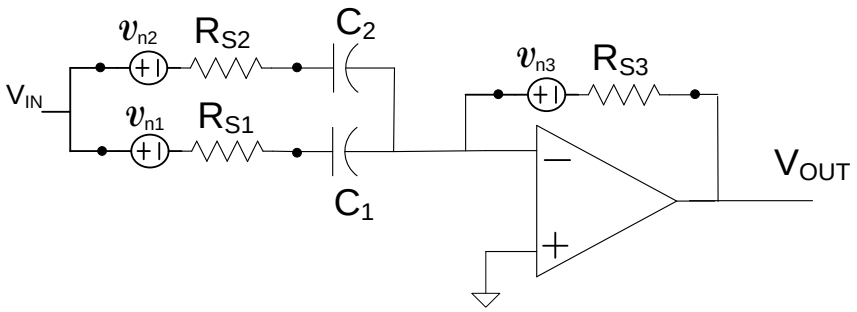
But noise is actually a bit worse than simply kT/C



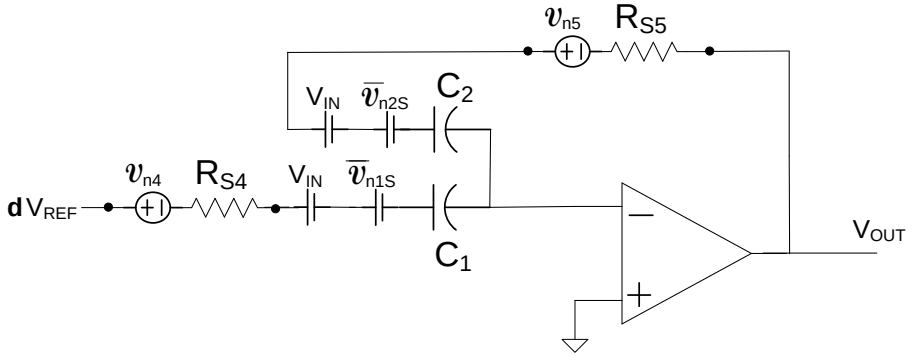
$$\beta_2 = \frac{C_2}{C_1 + C_2}$$

$$\beta_1 = 1$$

$$A_{FB2} = 1 + \frac{C_2}{C_1} = \frac{1}{\beta_2}$$

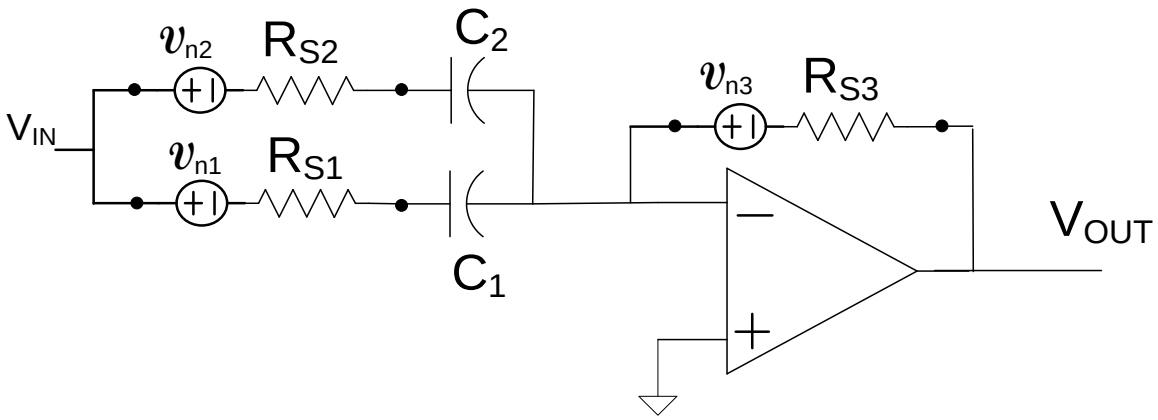


Track Mode



Hold Mode

Sampling Noise



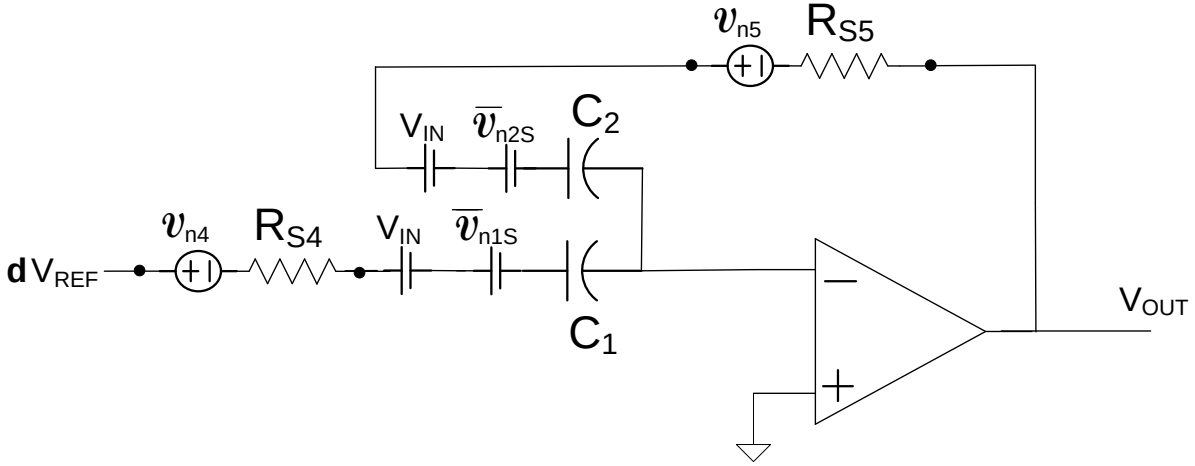
$\beta_1 = 1$

RMS Noise Voltage on capacitors C_1 and C_2

$$v_{n1_{RMS}} = \sqrt{\frac{kT}{C_1}} \quad \Rightarrow \quad \hat{v}_{n1_{RMS}} = \sqrt{\frac{kT}{C_1}}$$

$$v_{n2_{RMS}} = \sqrt{\frac{kT}{C_2}} \quad \Rightarrow \quad \hat{v}_{n2_{RMS}} = \sqrt{\frac{kT}{C_2}}$$

Sampling Noise



$$\beta_2 = \frac{C_2}{C_1 + C_2}$$

$$V_{OUT} = V_{IN}\left(\frac{1+\frac{C_2}{C_1}+sC_2(R_4+R_5)}{\frac{C_2}{C_1}+s\left[R_4C_2+\frac{1}{GB}\left(1+\frac{C_2}{C_1}\right)\right]+s^2\frac{1}{GB}(R_5+R_4)C_2}\right)$$

$$-\mathbf{d}_1 V_{REF}\left(\frac{1+R_5C_2s}{\frac{C_2}{C_1}+s\left[R_4C_2+\frac{1}{GB}\left(1+\frac{C_2}{C_1}\right)\right]+s^2\frac{1}{GB}(R_5+R_4)C_2}\right)$$

$$+\frac{\hat{V}_{n1}(1+R_5C_2s)+\hat{V}_{n2}\left(\frac{C_2}{C_1}(1+R_4C_1s)\right)}{\frac{C_2}{C_1}+s\left[R_4C_2+\frac{1}{GB}\left(1+\frac{C_2}{C_1}\right)\right]+s^2\frac{1}{GB}(R_5+R_4)C_2}$$

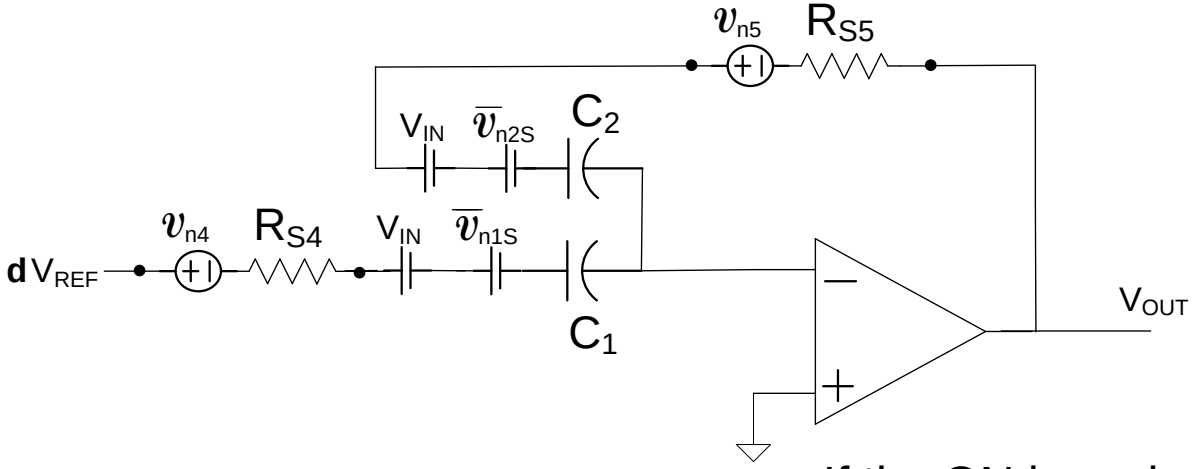
$$+\frac{\hat{v}_{n4}(1+R_5C_2s)-\hat{v}_{n5}\left(\frac{C_2}{C_1}(1+R_4C_1s)\right)}{\frac{C_2}{C_1}+s\left[R_4C_2+\frac{1}{GB}\left(1+\frac{C_2}{C_1}\right)\right]+s^2\frac{1}{GB}(R_5+R_4)C_2}$$

after settled only noise from R_{S4} and R_{S5} will be time varying

$$V_{OUT} = V_{IN}\left(1+\frac{C_1}{C_2}\right)-\mathbf{d}_1 V_{REF}\left(\frac{C_1}{C_2}\right)+\hat{V}_{n1}\left(\frac{C_1}{C_2}\right)+\hat{V}_{n2}$$

$$+\frac{\hat{v}_{n4}(1+R_5C_2s)-\hat{v}_{n5}\left(\frac{C_2}{C_1}(1+R_4C_1s)\right)}{\frac{C_2}{C_1}+s\left[R_4C_2+\frac{1}{GB}\left(1+\frac{C_2}{C_1}\right)\right]+s^2\frac{1}{GB}(R_5+R_4)C_2}$$

Sampling Noise



$$\beta_2 = \frac{C_2}{C_1 + C_2}$$

$$V_{OUT} = V_{IN}\left(1 + \frac{C_1}{C_2}\right) - d_1 V_{REF}\left(\frac{C_1}{C_2}\right) + \hat{V}_{n1}\left(\frac{C_1}{C_2}\right) + \hat{V}_{n2}$$

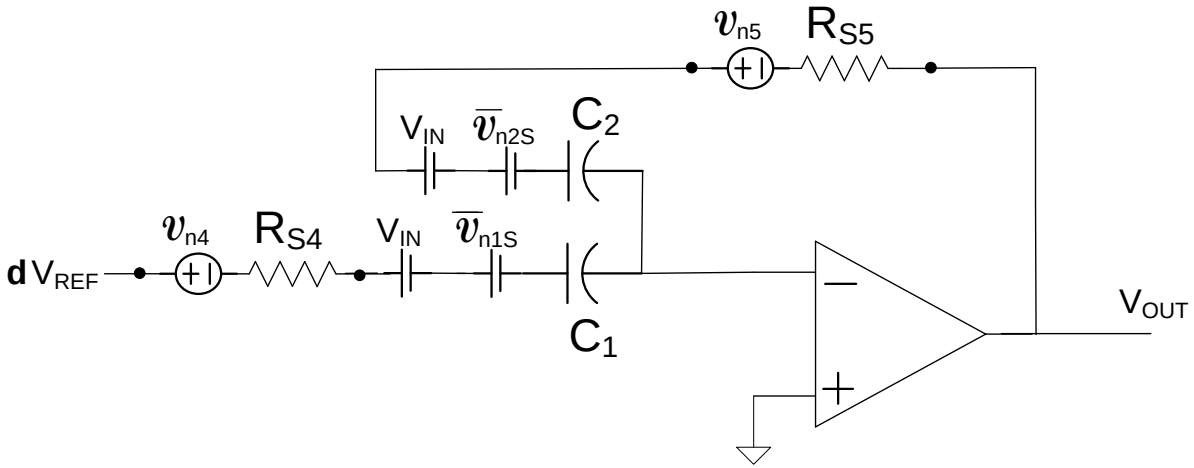
$$+ \frac{\hat{v}_{n4}(1 + R_5 C_2 s) - \hat{v}_{n5}\left(C_2/C_1\,(1 + R_4 C_1 s)\right)}{C_2/C_1 + s\left[R_4 C_2 + \frac{1}{GB}\left(1 + C_2/C_1\right)\right] + s^2 \frac{1}{GB}(R_5 + R_4) C_2}$$

If the ON impedance of the switches is small and C_1=C_2, it can be shown that output noise due to both switches is

$$v_{4\text{-}5RMS} = \sqrt{kTR_{SW}GB}$$

where R_{S4}=R_{S5}=R_{SW}

Sampling Noise



$$\beta_2 = \frac{C_2}{C_1 + C_2}$$

If the ON impedance of the switches is small and it is assumed that $C_1=C_2=C$, $R_{S4}=R_{S5}=R_{SW}$, it can be shown that noise on output is

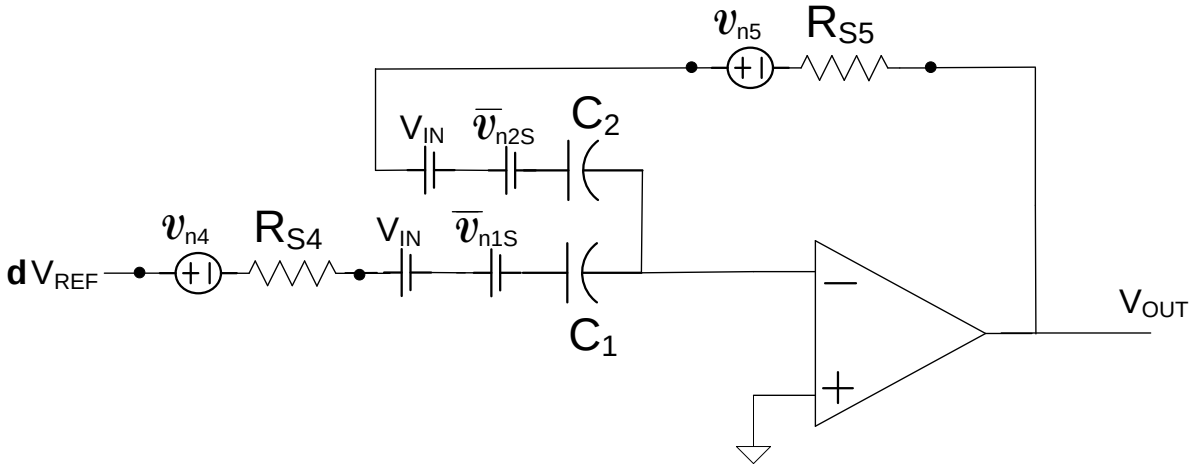
$$v_{4\text{-}5RMS} = \sqrt{kTR_4GB}$$

$$\hat{v}_{IN\text{-}RMS\phi_2} = \sqrt{\frac{2kT}{C} + kTR_4GB}$$

$$\hat{v}_{IN\text{-}RMS} = \sqrt{\frac{kT}{2C} + \frac{kTR_4GB}{4}}$$

We have now shown:

Sampling Noise



$$\beta_2 = \frac{C_2}{C_1 + C_2}$$

If the ON impedance of the switches is small and it is assumed that $C_1=C_2=C$, it can be shown that

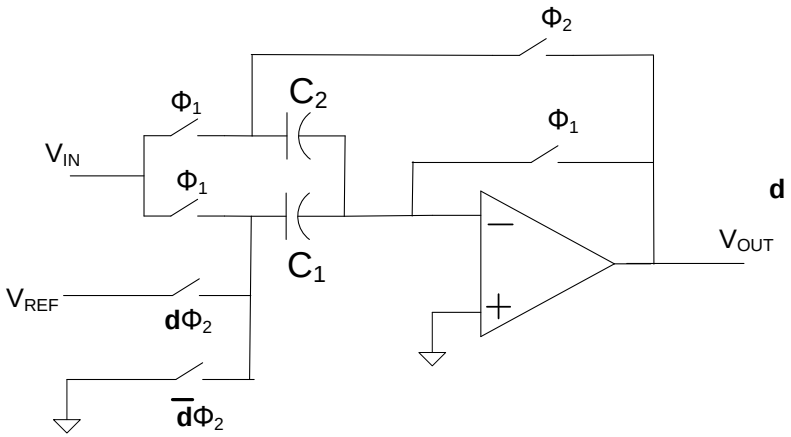
$$\hat{v}_{IN\text{-}RMS} = \sqrt{\frac{kT}{2C} + \frac{kTR_4GB}{4}}$$

Too much GB or too large of R_{SW} can increase sampled noise voltage

Too small of R_{SW} will not derive any benefit and will increase power, area, and driving problems

GB must be large enough to have complete settling

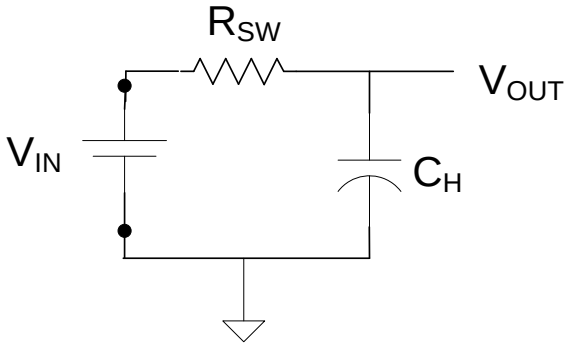
Switch Sizing

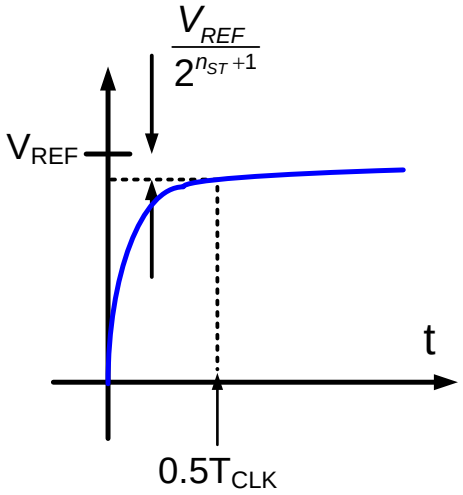


Sizing switches for constant input

Consider any first-order RC network

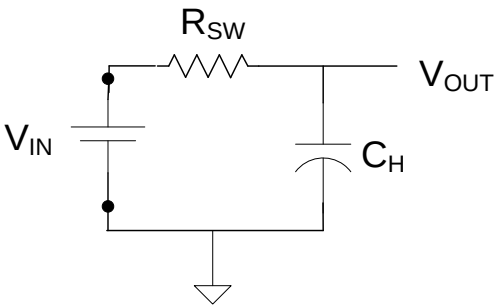
Target Settling: to ½ LSB in time $T_{CLK}/2$ for worst-case transition

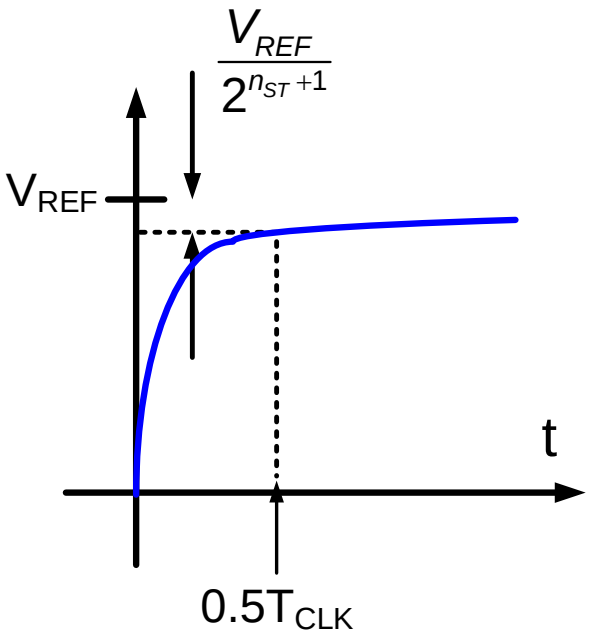




Switch Sizing

Target Settling: to ½ LSB in time $T_{CLK}/2$ for worst-case transition





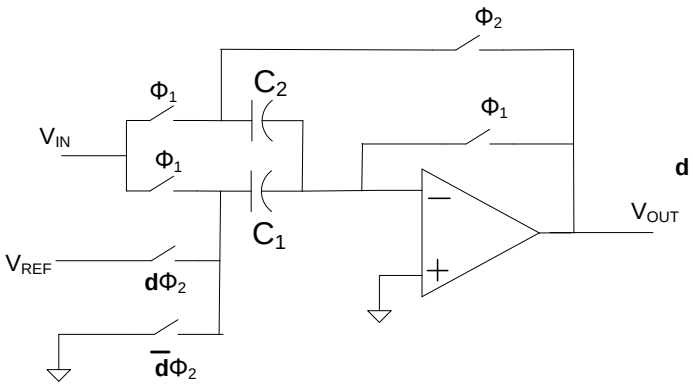
$$V_{REF}\left(1-e^{-\frac{t}{RC}}\right)=V_{REF}-V_{REF}\frac{1}{2^{n_{ST}+1}}$$

$$e^{-\frac{t}{RC}}=\frac{1}{2^{n_{ST}+1}}$$

$$R=\frac{t}{(n_{ST}+1)C\ln 2}$$

$$R_{SW}=\frac{1}{f_{CLK}(n_{ST}+1)C2\ln 2}$$

Switch Sizing



To settle to ½ LSB in time $T_{CLK}/2$

$$R_{SW} = \frac{1}{C_H f_{CLK} 2\ln(2)(n_{ST}+1)}$$

Recall minimum GB requirement (which is usually what will be designed for)

$$GB = \frac{(n_{ST}+1)2\ln 2}{\beta} f_{CLK}$$

Eliminating f_{CLK} we obtain

$$R_{SW} C_H = \frac{1}{\beta GB}$$

Define excess switch sizing factor θ by

$$R_{SW} = \frac{\theta}{C_H \beta GB}$$

Sampling Noise

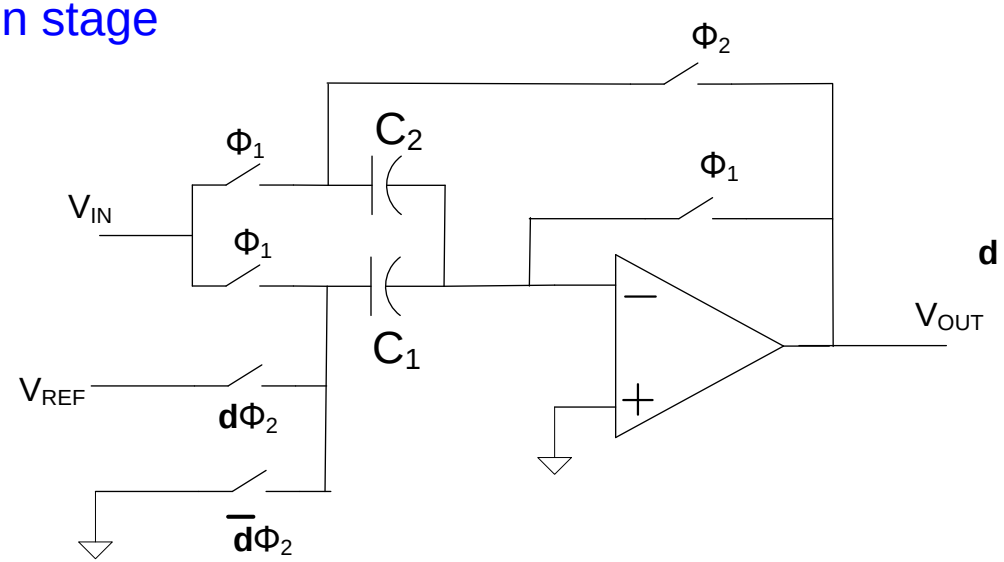
Summary of Flip-around SC gain stage

$$\beta_2 = \frac{C_2}{C_1 + C_2}$$

$$A_{FB} = 1 + \frac{C_1}{C_2}$$

$$\hat{v}_{IN\text{-}RMS} = \sqrt{\frac{kT}{C_1 + C_2} + \left(\frac{C_2}{C_1 + C_2}\right)^2 \hat{v}^2_{4\text{-}5RMS}}$$

$$R_4 = \frac{\theta}{C_1 \beta GB}$$



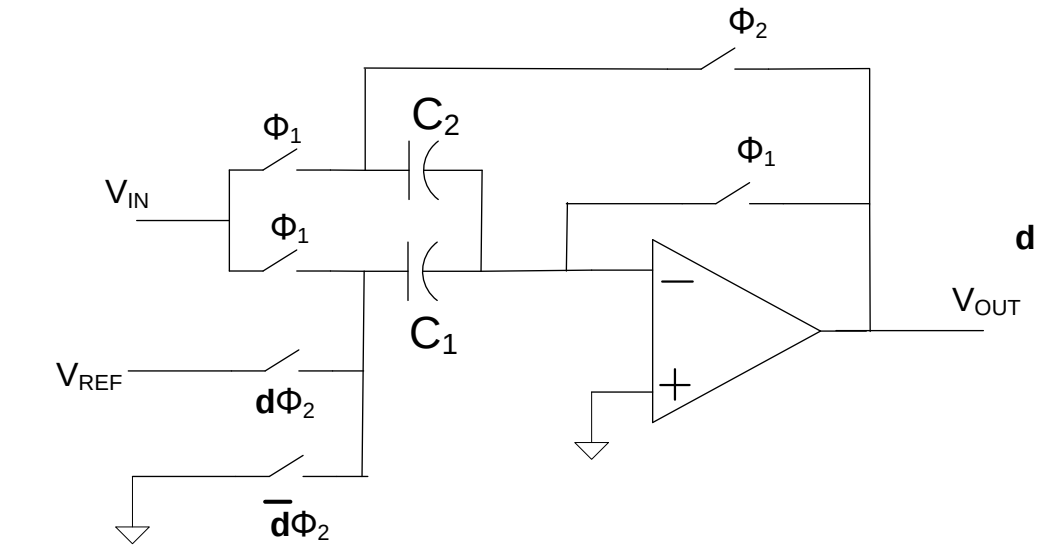
$$v_{4\text{-}5RMS} = \sqrt{2kT \frac{\theta}{C_1 \pi}\left(1 + \left(\frac{\beta}{1-\beta}\right)^2\right)} \sqrt{\int_{\omega=0}^{\infty} \frac{1 + \theta^2\omega^2}{\omega^4 (2\beta\theta)^2 + \omega^2\left(\left[\theta + \frac{\beta}{1-\beta}\right]^2 - \frac{4\theta\beta^2}{1-\beta}\right) + \left(\frac{\beta}{1-\beta}\right)^2} d\omega}$$

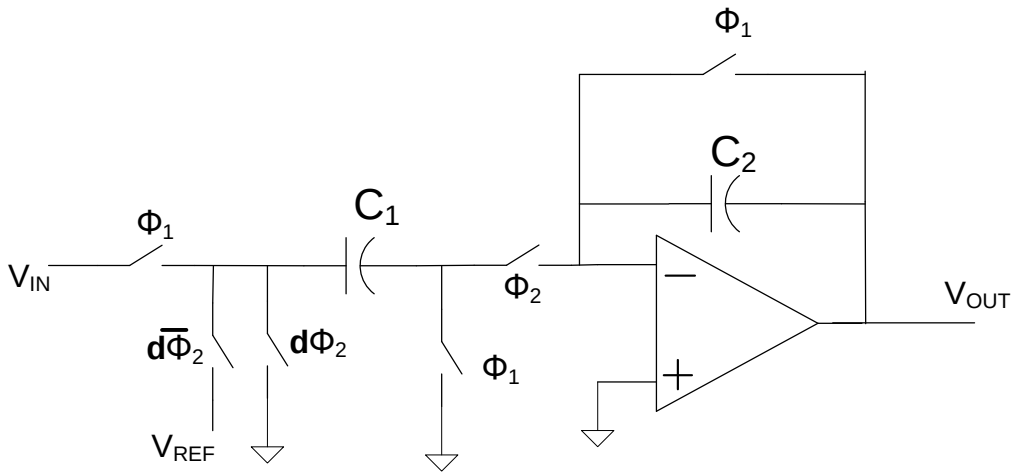
Often θ<<1 even with minimum sized devices and in this case $v_{4\text{-}5RMS}$ is negligible

$$\hat{v}_{IN\text{-}RMS} = \sqrt{\frac{kT}{C_1 + C_2}}$$

Sampling Noise

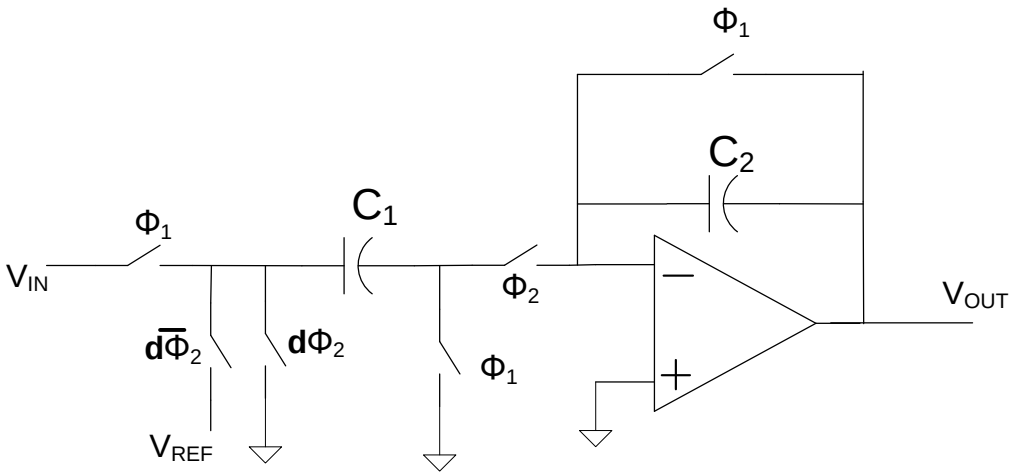
Two popular SC gain stages





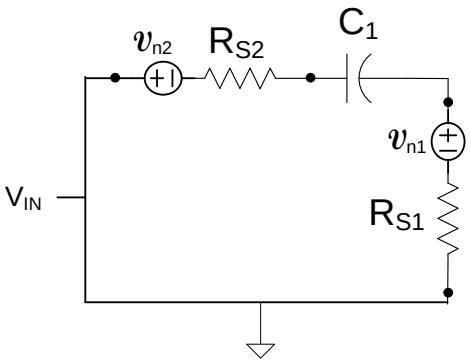
Sampling Noise

Basic SC gain stage

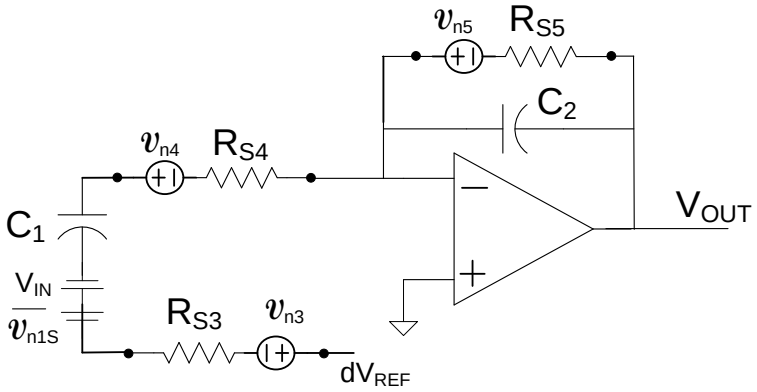


$$A_{FB} = -\frac{C_1}{C_2}$$

$$\beta = \frac{C_2}{C_1 + C_2}$$



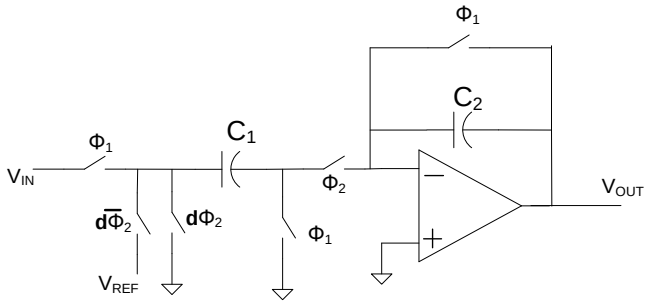
(a)

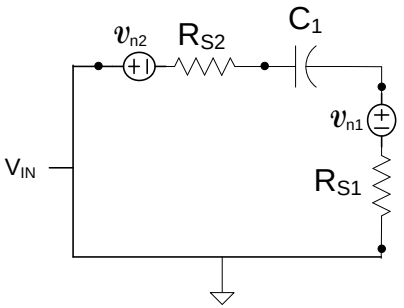


(b)

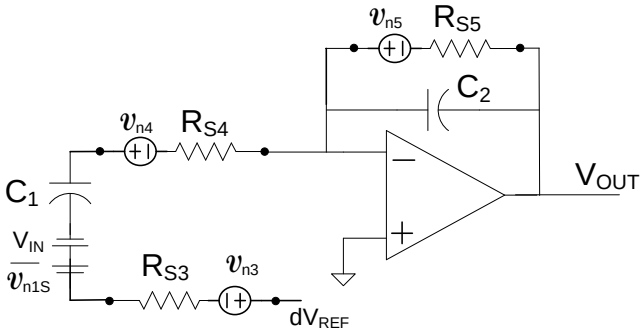
Sampling Noise

Basic SC gain stage





(a)



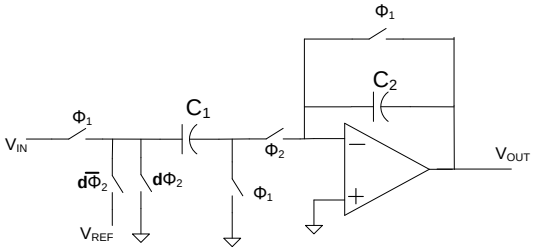
(b)

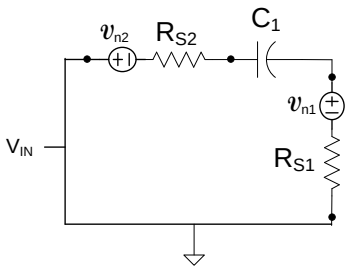
It can be shown that

$$V_{OUT} = \frac{C_1}{C_2}\left(V_{IN} + dV_{REF} + \vec{V}_{n1}\right) + V_{n4}\frac{C_1}{C_2}\left(\frac{1}{1 + R_4 C_1 s + \frac{s}{GB}\left(1 + \frac{C_1}{C_2} + R_4 C_1 s\right)}\right)$$

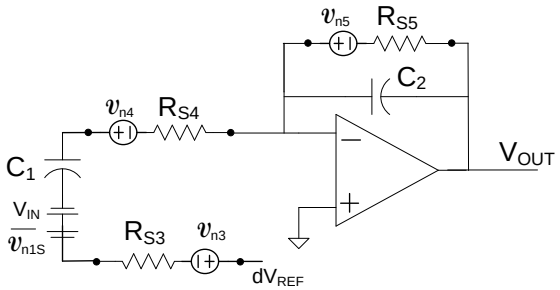
Sampling Noise

Basic SC gain stage





(a)



(b)

$$\beta=\frac{C_2}{C_1+C_2} \qquad R=\frac{\theta}{C_1\beta GB}$$

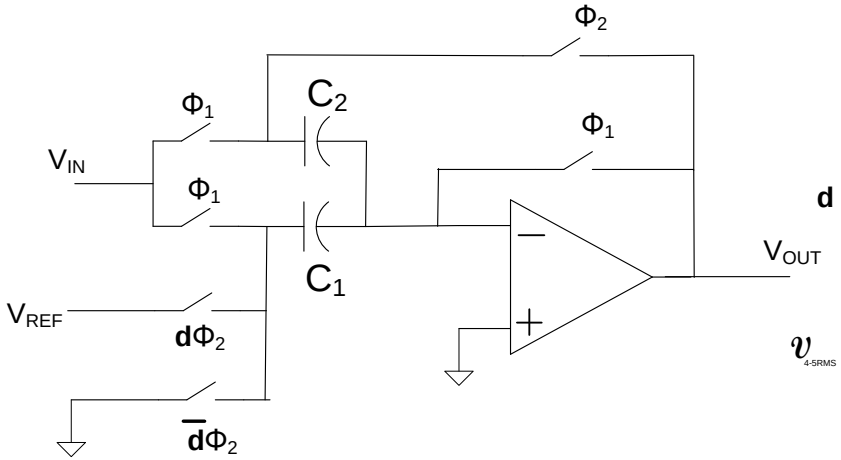
$$V_{OUT}=\frac{C_1}{C_2}\left(V_{IN}+dV_{REF}+\vec{V}_{n1}\right)+V_{n4}\frac{C_1}{C_2}\left(\frac{1}{1+R_4C_1s+\frac{s}{GB}\left(1+\frac{C_1}{C_2}+R_4C_1s\right)}\right)$$

$$v_{OUTn4RMS}=\sqrt{\frac{2kT\theta}{C_1\pi}\left(\frac{1-\beta}{\beta}\right)^2\int_{\omega=0}^{\infty}\left|\frac{1}{1+\omega^2\left[(1+\theta)^2-2\theta\beta\right]+\omega^4(\theta\beta)^2}\right|^2 d\omega}$$

$$\hat{v}_{IN\text{-}RMS}=\sqrt{\frac{kT}{C_1}+\left(\frac{C_2}{C_1}\right)^2\hat{v}^2_{OUT4\text{-}RMS}} \qquad \theta<<1 \qquad \hat{v}_{IN\text{-}RMS}=\sqrt{\frac{kT}{C_1}}$$

Sampling Noise

Two popular SC gain stages



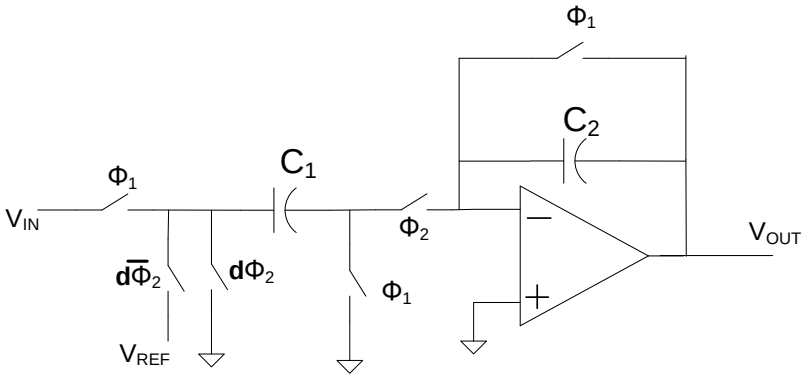
$$A_{FB} = 1 + \frac{C_1}{C_2} \qquad \beta_2 = \frac{C_2}{C_1 + C_2}$$

$$\hat{v}_{IN\text{-}RMS} = \sqrt{\frac{kT}{C_1 + C_2} + \left(\frac{C_2}{C_1 + C_2}\right)^2 \hat{v}^2_{4\text{-}5RMS}}$$

$$v_{4\text{-}5RMS} = \sqrt{2kT\frac{\theta}{C_1\pi}\left(1+\gamma\left(\frac{\beta}{1-\beta}\right)^2\right)}\sqrt{\int_{\omega=0}^{\infty} \frac{1+\theta^2\omega^2}{\omega^4(2\beta\theta)^2 + \omega^2\left(\left[\theta+\frac{\beta}{1-\beta}\right]^2 - \frac{4\theta\beta^2}{1-\beta}\right) + \left(\frac{\beta}{1-\beta}\right)^2} d\omega}$$

$\theta << 1$

$$\hat{v}_{IN\text{-}RMS} = \sqrt{\frac{kT}{C_1 + C_2}}$$



$$A_{FB} = -\frac{C_1}{C_2} \qquad \beta = \frac{C_2}{C_1 + C_2}$$

$$\hat{v}_{IN\text{-}RMS} = \sqrt{\frac{kT}{C_1} + \left(\frac{C_2}{C_1}\right)^2 \hat{v}^2_{OUT4\text{-}RMS}}$$

$$v_{OUTn4RMS} = \sqrt{\frac{2kT\theta}{C_1\pi}\left(\frac{1-\beta}{\beta}\right)^2 \int_{\omega=0}^{\infty} \left|\frac{1}{1+\omega^2\left[(1+\theta)^2 - 2\theta\beta\right] + \omega^4(\theta\beta)^2}\right|^2 d\omega}$$

$\theta << 1$

$$\hat{v}_{IN\text{-}RMS} = \sqrt{\frac{kT}{C_1}}$$

Sampling Noise

When is the continuous-time SC noise really of concern?

Recall

$$GB = \frac{(n_{ST}+1)2\ln 2}{\beta} f_{CLK}$$

$$\sqrt{\frac{kT}{C}} = \frac{1V}{2^{n+1}}$$

$$R_4 = \frac{1}{C_1 \beta GB}$$

Eliminating GB and C

$$R_4 = \frac{1}{kT 2^{2n_{ST}+2} (n_{ST}+1) 2\ln 2 f_{CLK}}$$

Sampling Noise

When is the continuous-time SC noise really of concern?

$$R_{MAX} = \frac{1}{kT2^{2n_{ST}+2}\left(n_{ST}+1\right)2\ln 2 f_{CLK}}$$

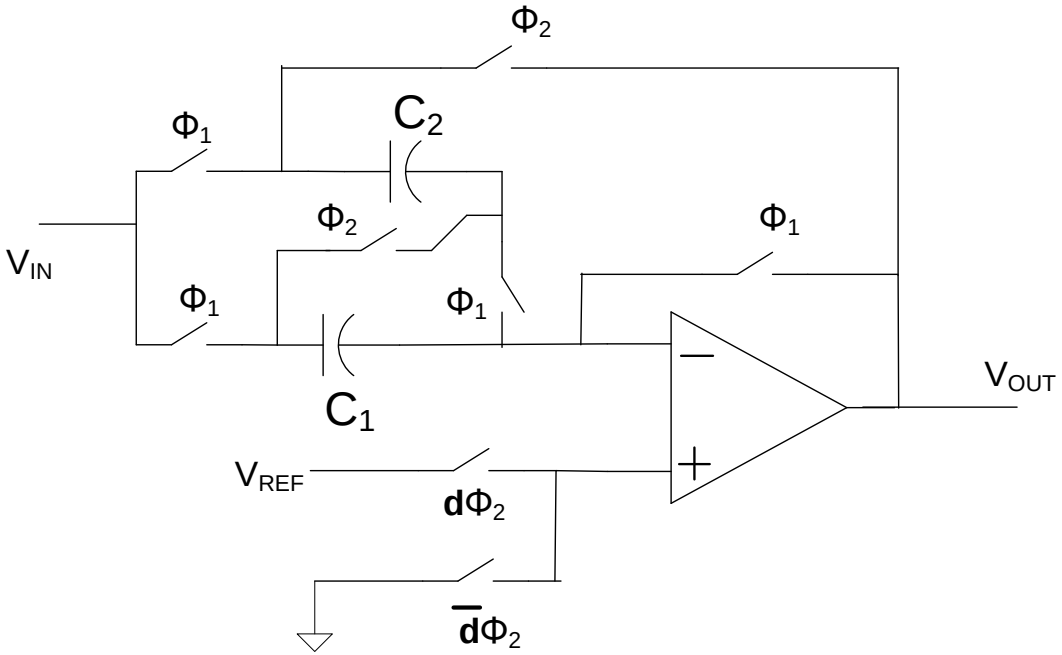
$R_{MAX}(fCLK,n)$

Clock Speed

Resolution	10	100	1K	10K	100K	1M	10M	100M	1G
4	4.7E+15	4.7E+14	4.7E+13	4.7E+12	4.7E+11	4.7E+10	4.7E+09	4.7E+08	4.7E+07
5	9.8E+14	9.8E+13	9.8E+12	9.8E+11	9.8E+10	9.8E+09	9.8E+08	9.8E+07	9.8E+06
6	2.1E+14	2.1E+13	2.1E+12	2.1E+11	2.1E+10	2.1E+09	2.1E+08	2.1E+07	2.1E+06
7	4.6E+13	4.6E+12	4.6E+11	4.6E+10	4.6E+09	4.6E+08	4.6E+07	4.6E+06	4.6E+05
8	1.0E+13	1.0E+12	1.0E+11	1.0E+10	1.0E+09	1.0E+08	1.0E+07	1.0E+06	1.0E+05
9	2.3E+12	2.3E+11	2.3E+10	2.3E+09	2.3E+08	2.3E+07	2.3E+06	2.3E+05	2.3E+04
10	5.2E+11	5.2E+10	5.2E+09	5.2E+08	5.2E+07	5.2E+06	522353.4	52235.3	5223.5
11	1.2E+11	1.2E+10	1.2E+09	1.2E+08	1.2E+07	1.2E+06	119706	11970.6	1197.1
12	2.8E+10	2.8E+09	2.8E+08	2.8E+07	2.8E+06	2.8E+05	27624.46	2762.4	276.2
13	6.4E+09	6.4E+08	6.4E+07	6412821	641282.1	64128.21	6412.821	641.3	64.1
14	1.5E+09	1.5E+08	1.5E+07	1496325	149632.5	14963.25	1496.3	149.63	14.96
15	3.5E+08	3.5E+07	3.5E+06	350701.2	35070	3507	350.7	35.07	3.51
16	8.3E+07	8.3E+06	8.3E+05	82517.92	8252	825	82.51792	8.25	0.83
17	1.9E+07	1.9E+06	194834	19483.4	1948	195	19.4834	1.94834	0.194834
18	4.6E+06	4.6E+05	46144.89	4614.5	461.4	46.1	4.614489	0.461449	0.046145
19	1.1E+06	109594.1	10959.41	1095.9	109.6	11.0	1.095941	0.109594	0.010959
20	2.6E+05	26093.84	2609.384	260.9384	26.09384	2.609384	0.260938	0.026094	0.002609

Sampling Noise

What about this one?

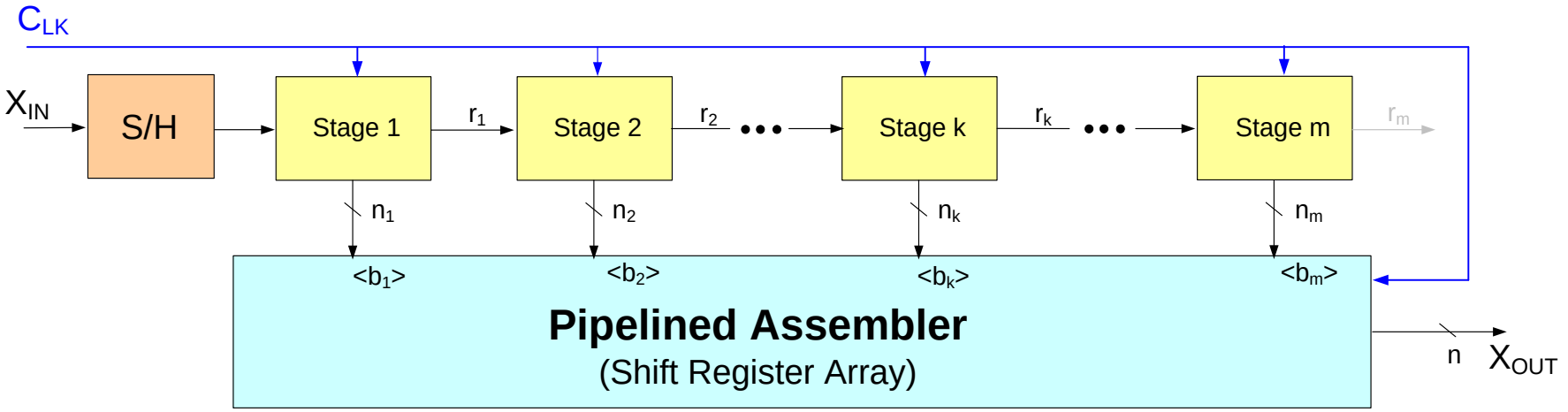


A_{FB}=?

β=?

Series-Parallel Structure

Sampling Noise



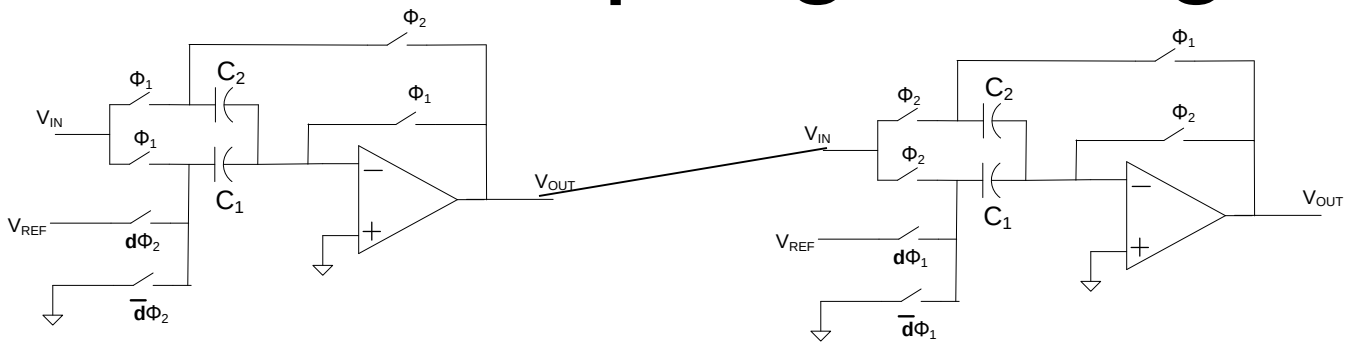
Sampling noise from all stages must be referred back to input !

$$v^2_{INRMS} = v^2_{IN1} + \frac{1}{A_1^2} v^2_{IN2} + \frac{1}{A_1^2 A_2^2} v^2_{IN3} + \ldots + \frac{1}{A_1^2 A_2^2 \cdots A_{n-1}^2} v^2_{INn}$$

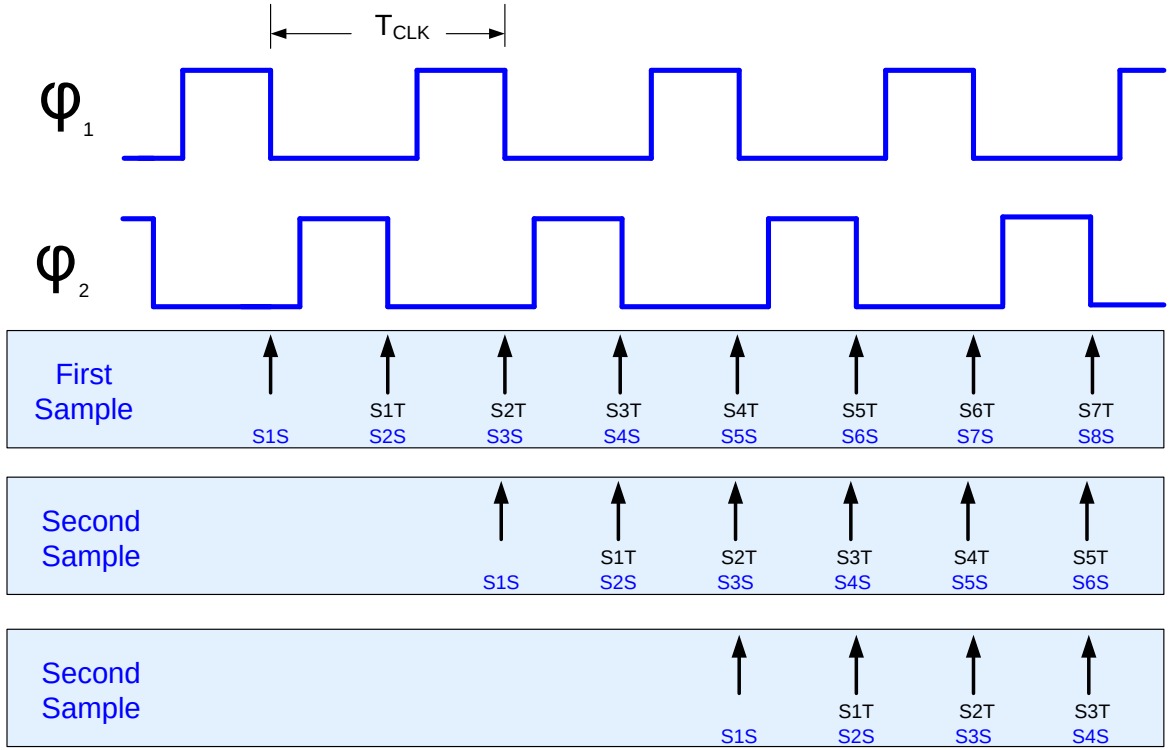
$$v_{INRMS} = \sqrt{v^2_{IN1} + \sum_{k=2}^{n} \left(\frac{v_{INk}}{\prod_{i=1}^{k-1} A_i} \right)^2}$$

See Katyal,Lin and Geiger, ISCAS, for capacitor sizing for minimization of noise and power

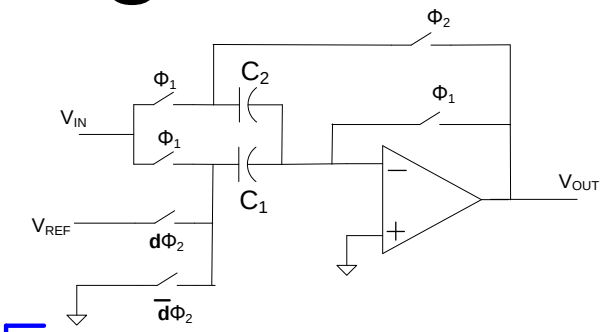
Sampling Timing

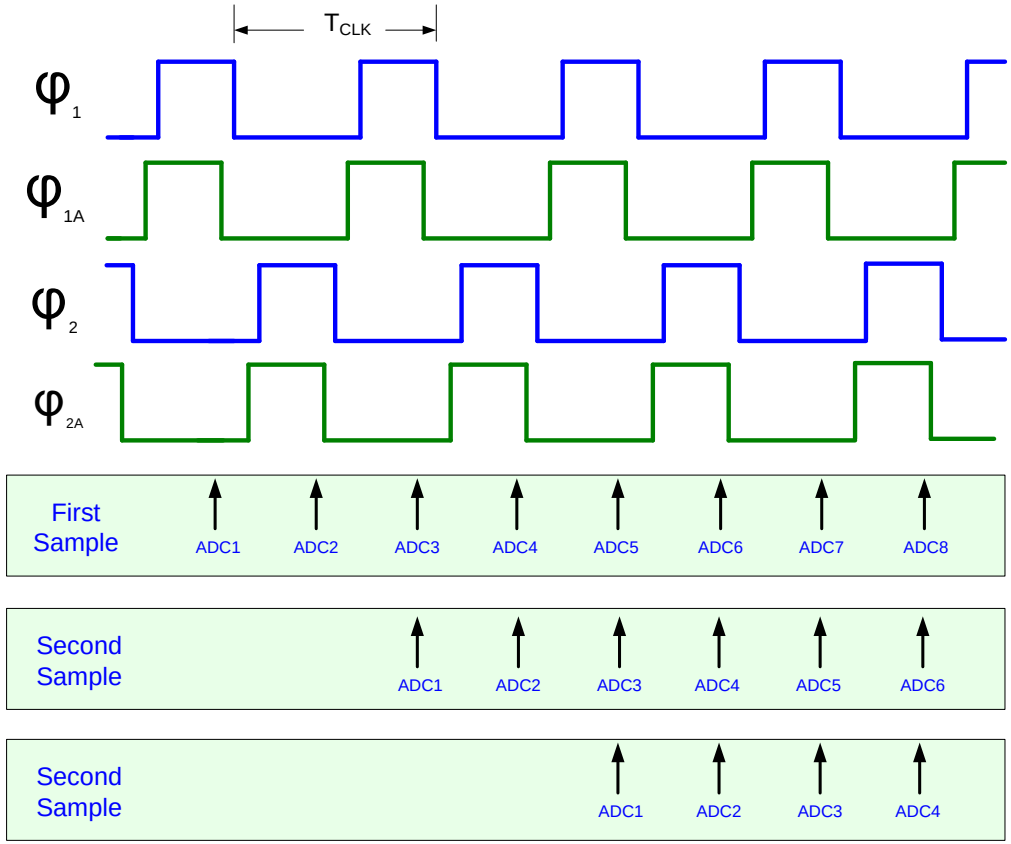


Even numbered stages sampled with φ_1 and odd stages sampled with φ_2



Sampling Timing





Quiet sampling is important

Pipelined Data Converter Design Guidelines

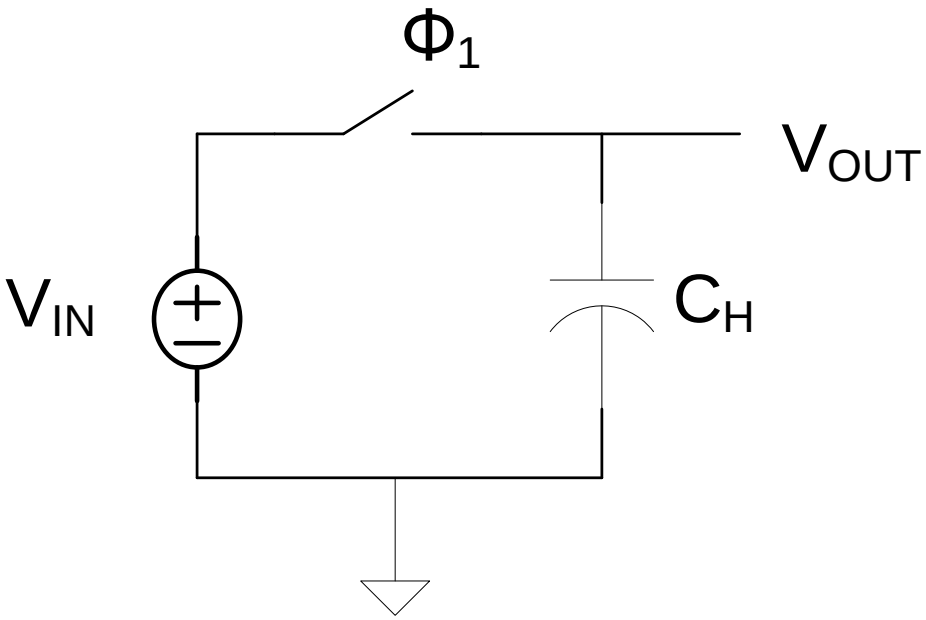
Issue	Strategy
1. ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	1. Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if α_k's correctly interpreted a) Use Extra Comparators b) Use sub-radix structures
2. Op Amp Gain causes finite gain errors and introduces noninearity	2. a) Select op amp architecture that has acceptable signal swing b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors
3. Op amp settling must can cause errors	3. Select GB to meet settling requirements (degrade modestly to account for slewing)
4. Power dissipation strongly dependent upon GB of Op Amps	4. Minimize C_L, use energy efficient op amps, share or shut down op amp when not used,scale power in latter stages, eliminate input S/H if possible, interleave at high frequencies. Good (near optimal) noise distribution strategy should be followed.
5. Choice of FB Amplifier Architecture seriously impacts performance	5. Bottom plate sampling, bootatrapping, clock advance to reduce aperature uncertainty,critical GB, parasitic insensitivity needed, β dependent upon architecture and phase, compensation for worst-case β, TG if needed
6. Correct interpretation of α_k's is critical	6. a) Accurately set α_k values b) Use analog or digital calibration

Pipelined Data Converter Design Guidelines

	Issue	Strategy
7.	Sampling operation inherently introduces a sampled-noise due to noise in resistors	Select the capacitor sizes to meet noise requirements. Continuous-time noise can also be present but is often dominated by sampled noise. Size switches to meet settling and noise requirements. Excessive GB will cause noise degradation in some applications, include noise from all stages (not just first stage) .

Bootstrapped Switch

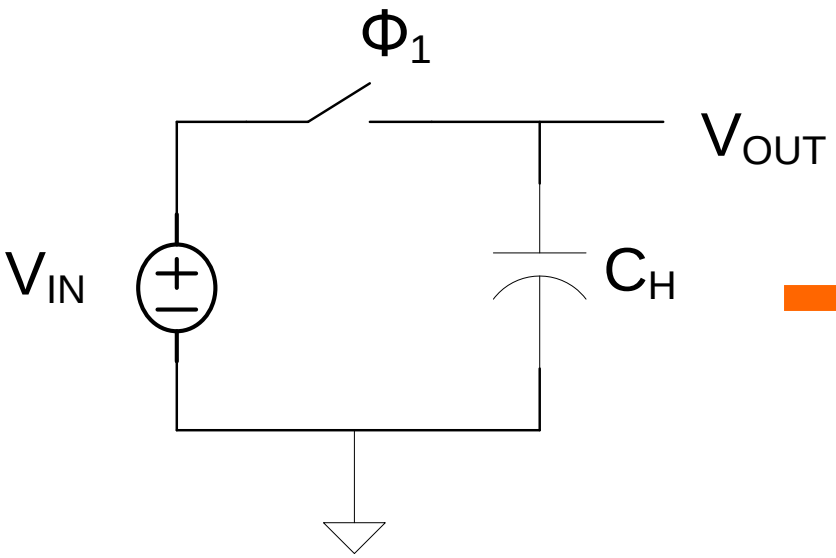
The ideal sampling operation



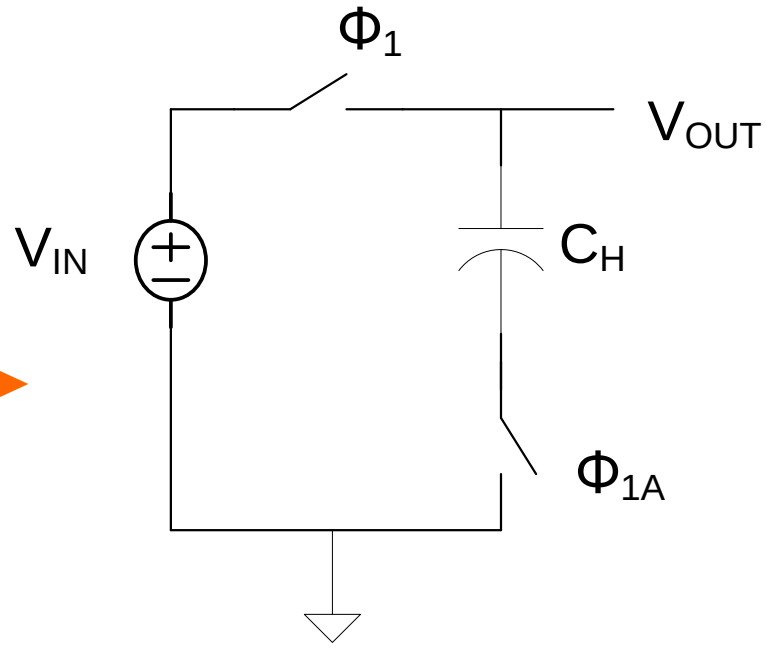
Should track V_{IN} in the TRACK mode
Should accurately sample V_{IN} at transition to HOLD mode

Bootstrapped Switch

The ideal sampling operation



Single V_{IN}-referenced switch

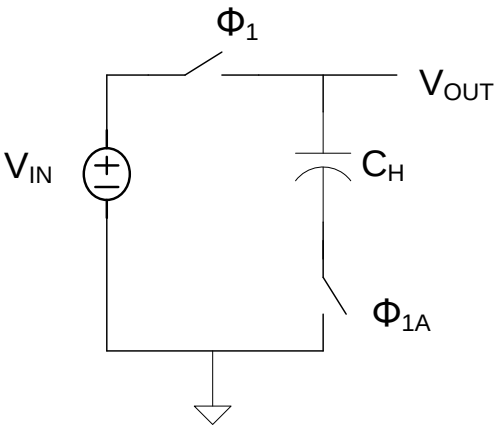


Bottom plate sampling

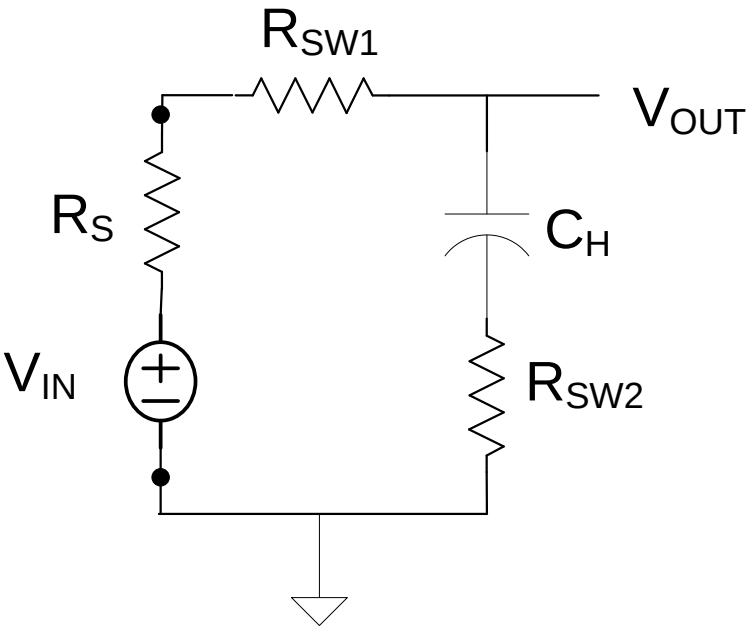
Should track V_{IN} in the TRACK mode
Should accurately sample V_{IN} at transition to HOLD mode

Bootstrapped Switch

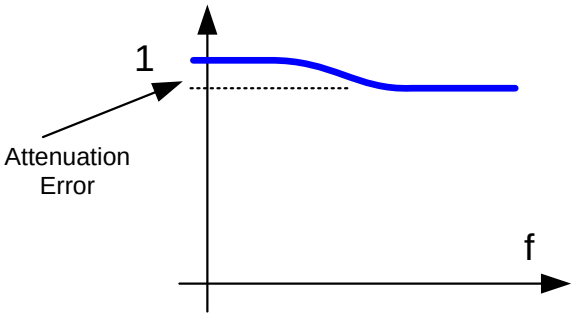
The ideal sampling operation



If linear



$$\frac{V_{OUT}}{V_{IN}} = \frac{1+R_{SW2}C_L s}{1+(R_S+R_{SW1}+R_{SW2})C_L s}$$



For high frequency inputs, an attenuation error will occur

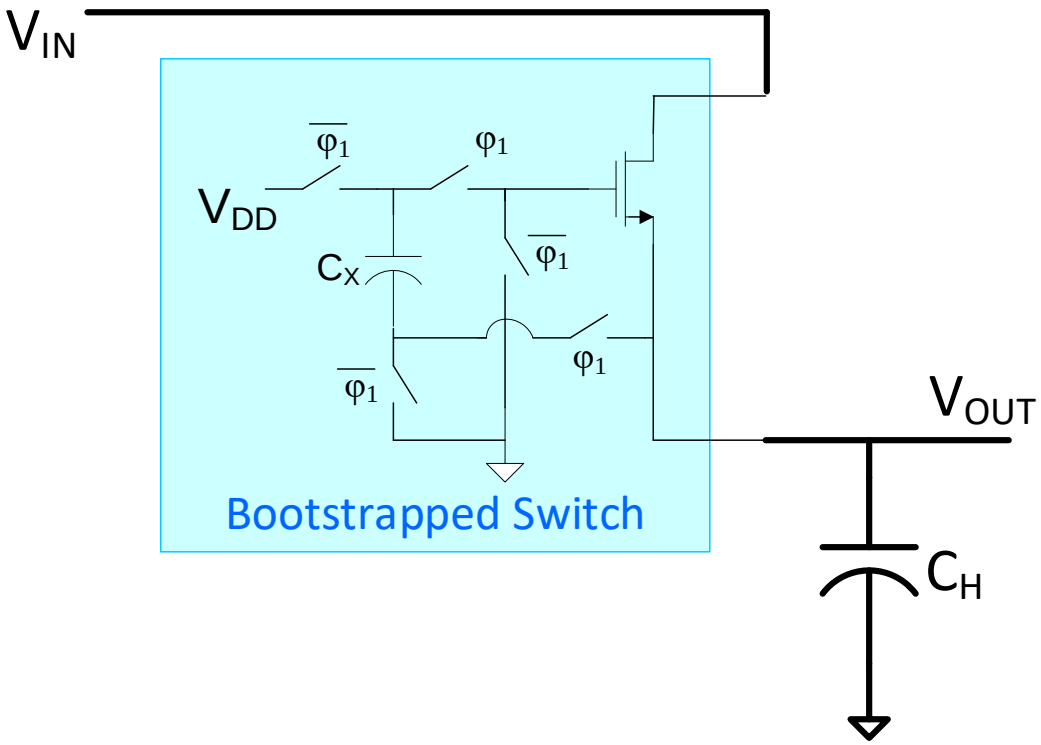
Affects absolute accuracy but not linearity

But, if switches are nonlinear, will introduce a nonlinear error that can be very substantial

Signal dependent R_{SW} or switch nonlinearity will introduce nonlinear errors

Bootstrapped Switch

Bootstrapping Principle



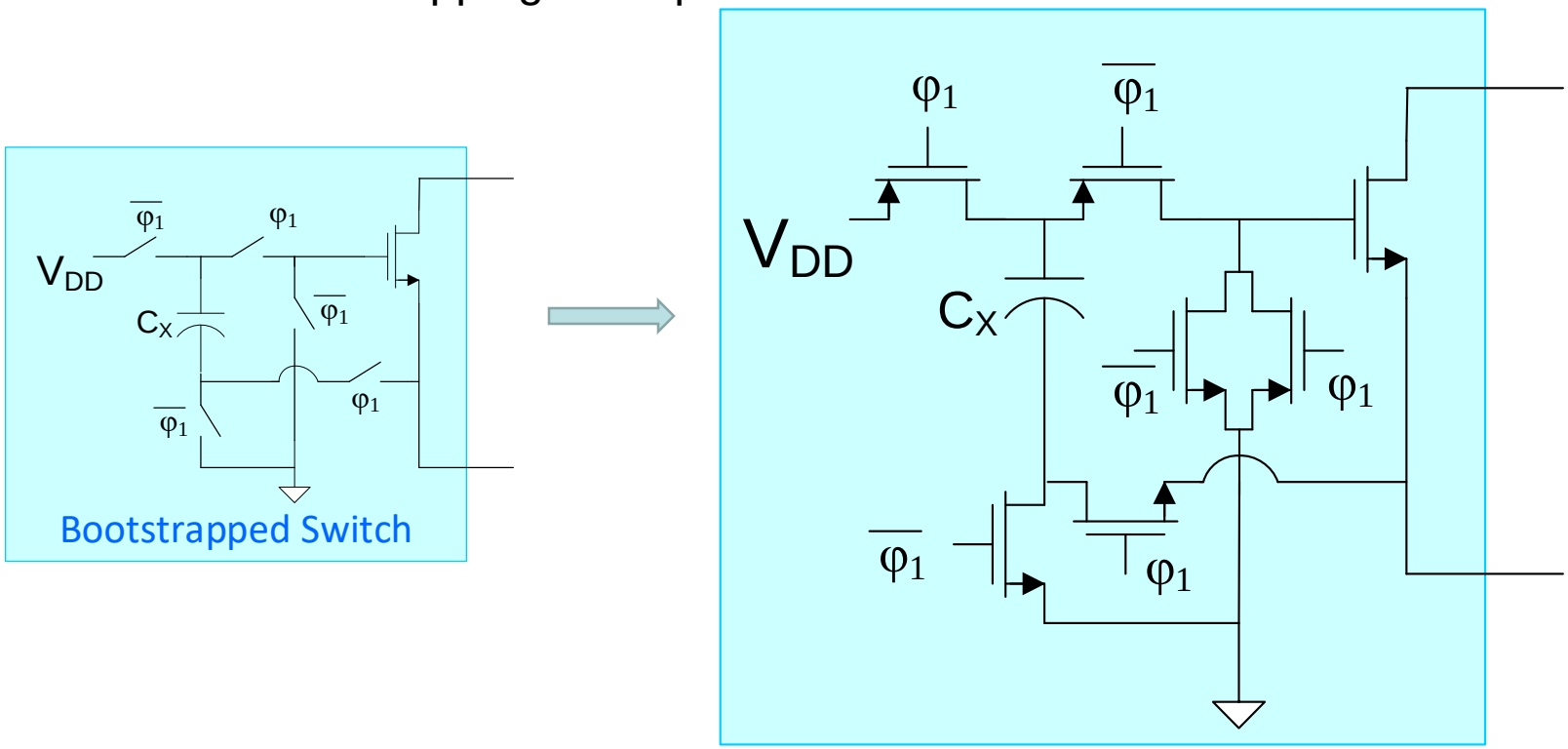
During phase $\overline{\phi}_1$ C_X is charged to V_{DD} and MOS switch is OFF

During phase ϕ_1 C_X is placed across V_{GS} and MOS switch is ON

With bootstrapping, R_{SW} is independent of V_{IN}

Bootstrapped Switch

Bootstrapping Principle

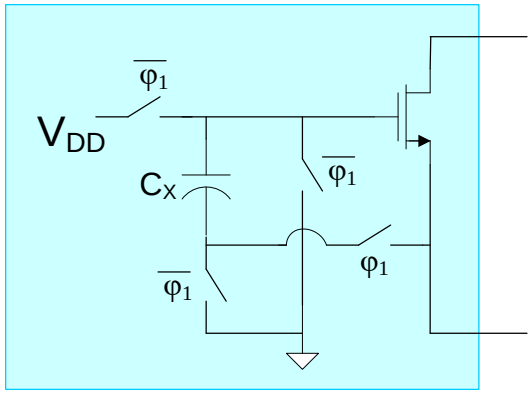


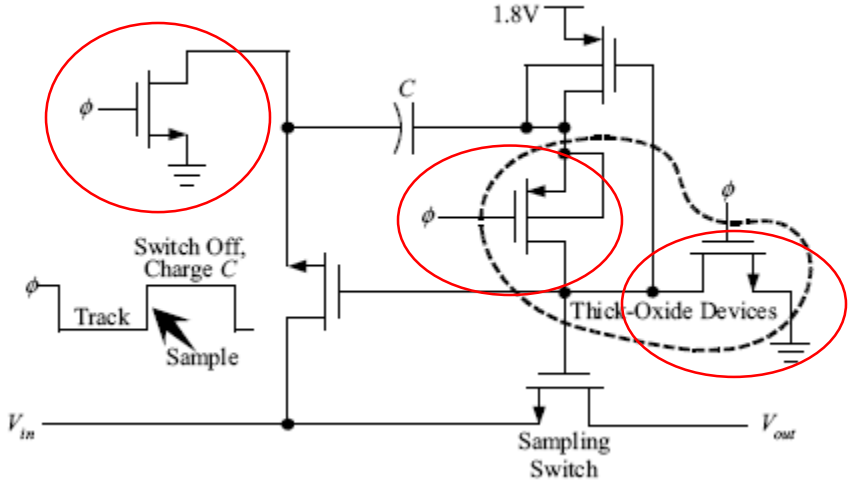
Conceptual Realization

- May have difficult time turning on some switches
- May stress gate oxide !

Bootstrapped Switch

Bootstrapping Principle



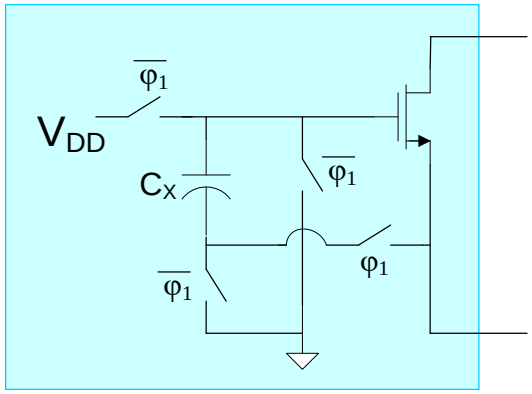


From Galton, ISSCC 04

Note: Signal does not affect turn-on time or voltage of sampling switches (all relative to VDD or GND)

Bootstrapped Switch

Bootstrapping Principle



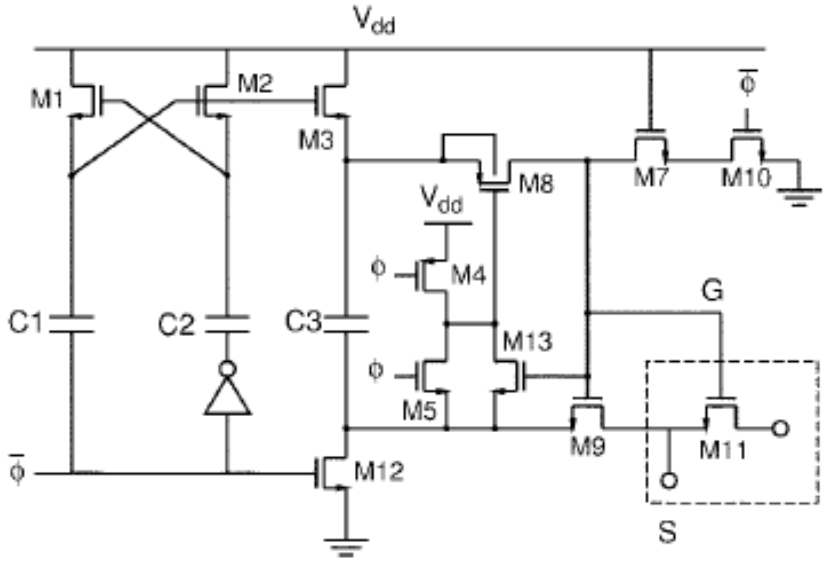
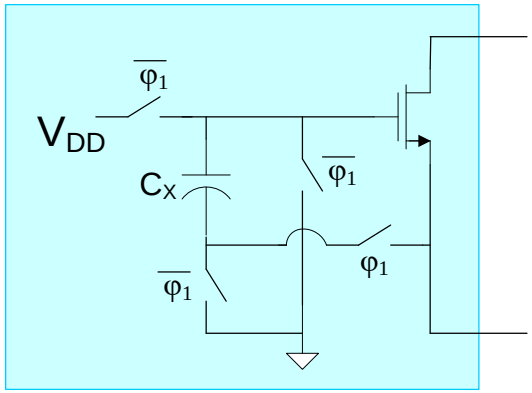


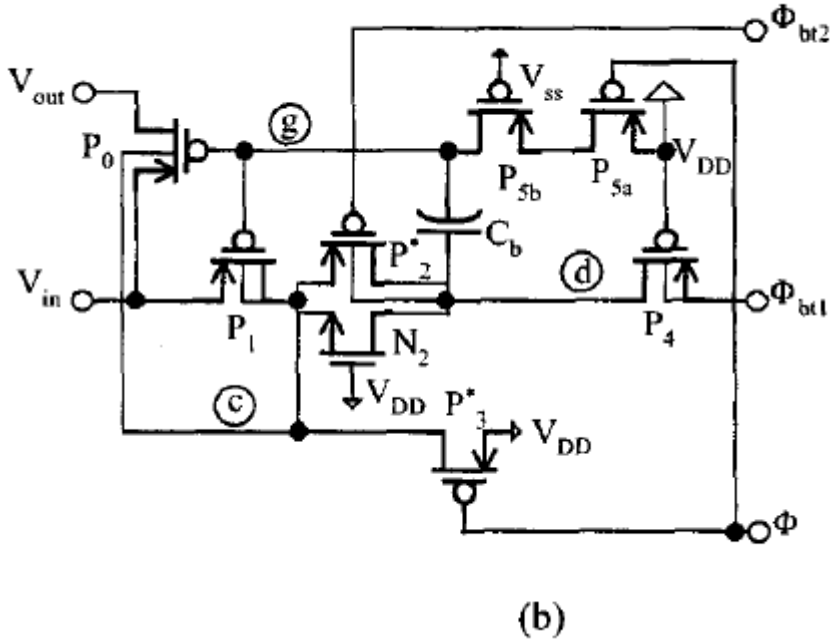
Fig. 7. Bootstrap circuit and switching device.

From Abo and Gray JSC 99

Bootstrapped Switch

Bootstrapping Principle



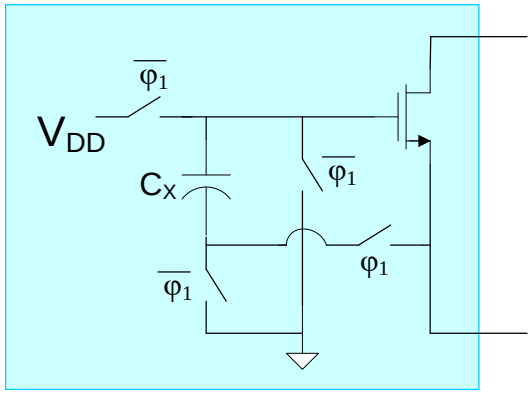


(b)

From Roberts MWSCAS 2000

Bootstrapped Switch

Bootstrapping Principle



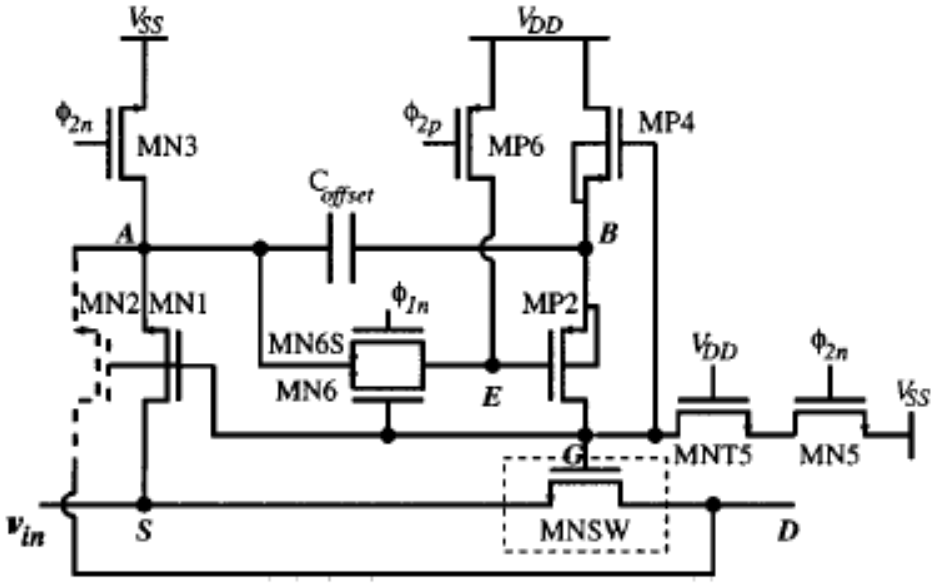
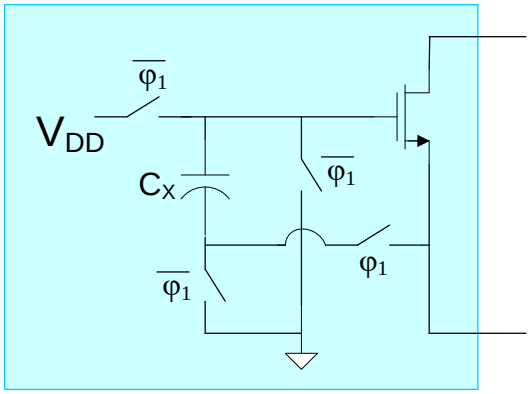


Fig. 7. Transistor-level implementation of the bootstrapped switch.

From Kaiser JSC 2001

Bootstrapped Switch

Bootstrappi



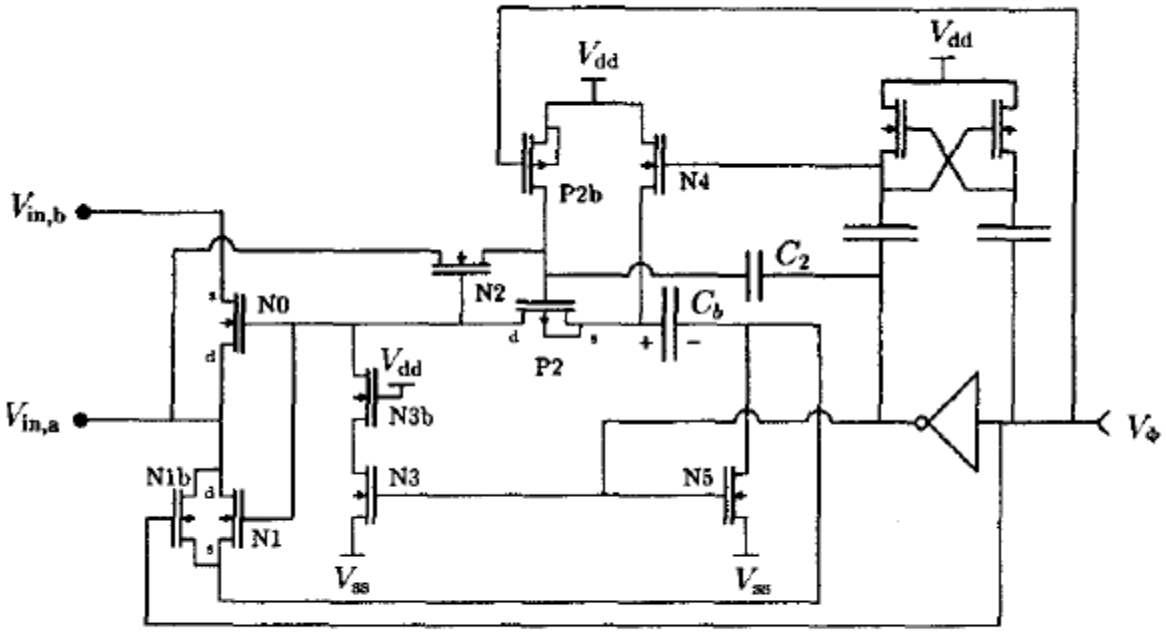


Figure 5: Bootstrapped switch.

From Steensgaard ISCAS 1999

Pipelined Data Converter Design Guidelines

Issue	Strategy
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Pipelined Data Converter Design Guidelines

	Issue	Strategy
7.	Sampling operation inherently introduces a sampled-noise due to noise in resistors	Select the capacitor sizes to meet noise requirements. Continuous-time noise can also be present but is often dominated by sampled noise. Size switches to meet settling and noise requirements. Excessive GB will cause noise degradation in some applications, include noise from all stages (not just first stage) .
8.	Signal-dependent tracking errors at input introduce linearity degradation	Bootstrapped switches almost always used at input stage. Must avoid stressing oxide on bootstrapped switches

End of Lecture 26